Designing High Power Parallel Arrays with PRMs™

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Introduction

VI Chip® PRM™ Regulators and VTM™ Current Multipliers can be configured in parallel to allow for greater system power capacity. When PRMs and VTMs are connected in parallel, the array can support higher current and power than a circuit with a single PRM and VTM, taking efficiency derating and other factors into account. This note discusses PRM types that can be used both in Adaptive Loop and Remote Sense and considerations when using them in parallel.

In Adaptive-Loop operation, the PRM uses its internal-control loop to respond to changes to the PRM's output voltage and its temperature. In Remote Sense operation, the PRM relies on external circuitry to sense output current and the load voltage. Parallel arrays retain both of these operating modes. Some additional circuitry and design considerations are needed in parallel configurations. For simplicity, Adaptive-Loop Arrays are covered first (see Arrays for Adaptive-Loop / Parent-Child Operation), then Remote Sense Arrays (see Arrays for Remote Sense Operation).

Additional topics such as redundancy and board-to-board arrays, are beyond the scope of this document, but may be possible with more advanced techniques. Please contact Vicor Applications Engineering for additional information.

Arrays for Adaptive-Loop / Parent-Child Operation

In an Adaptive-Loop Array, PRMs are configured as a parent and several children. The parent PRM implements the active control loop, which uses control pin inputs to drive the SHARE pin to the child PRMs.

Up to five PRMs of the same type may be placed in parallel with minimal additional circuitry. More PRMs can be placed in parallel through the use of external circuitry; the implementation of the additional circuitry depends on the system requirements.

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Figure 1
PRM™ – VTM™ Array,
Adaptive Loop

Figure 1
PRM™ – VTM™ Array,
Adaptive Loop
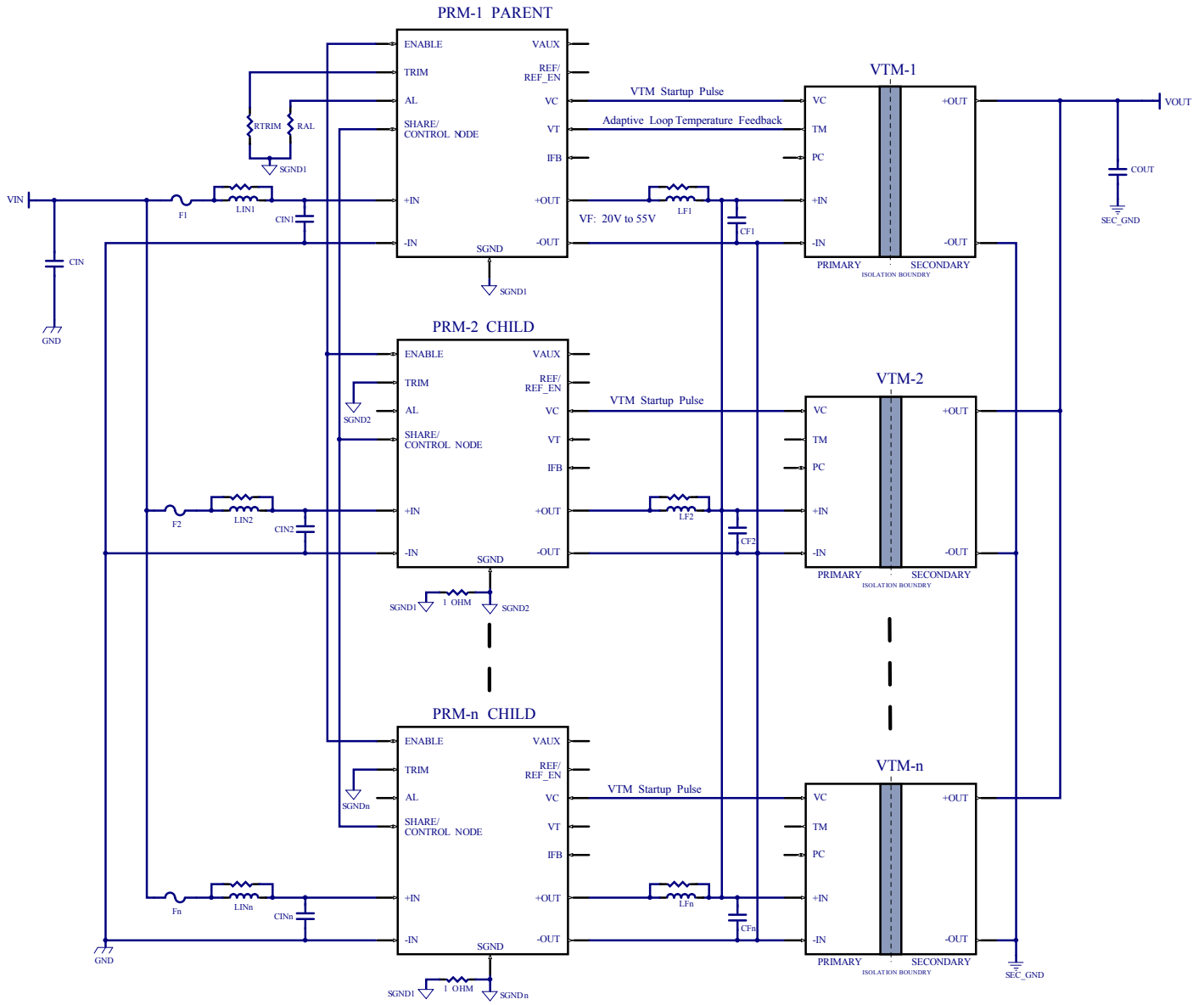
High-Level Guidelines for Adaptive-Loop Operation

The following high-level guidelines must be followed in order for an Adaptive-Loop supply to start up and operate properly to avoid overstress and stay within the absolute maximum ratings.

- An independent fuse for each PRM +IN connection is required to maintain safety certifications.

- All PRMs in the array must be powered from a common power source so that the input voltage to each PRM is the same. The –IN pins of all PRMs must be connected together. An independent inductor for each PRM +IN and +OUT connection is required when used in an array to control circulating currents among the PRMs and reduce the impact of beat frequencies.

- ENABLE pins must be connected together for start-up synchronization and proper fault response of the array.

- One PRM™ must be designated as a parent through configuring the TRIM pin voltage within the recommended range.

- All other PRMs must be designated as child PRMs by tying TRIM pins to SGND. Vicor recommends making this connection through a 0Ω jumper for troubleshooting purposes.

- SHARE pins must be connected together to enable sharing. The bandwidth requirements of SHARE are low enough that the bus can be considered a lumped element rather than a transmission line and so star connections to the parent PRM with stubs, as well as daisy-chain connections are permitted.

- To avoid introducing additional noise, the SHARE trace length between devices should be minimized and the SHARE bus should not be routed under any PRM.

- SGND of the parent PRM is the reference for all control-loop functions. The SGND pins of each child PRMs should be connected to the SGND reference node on the board through a 1Ω resistor.

- When operating within an array the parent PRM is rated for full power while the child PRMs are derated to the power and current values provided for Child operation (P_{OUT_ARRAY}, I_{OUT_ARRAY} – refer to PRM data sheet). The number of PRMs required to achieve a given array capacity must take these deratings into account to avoid overstressing the PRMs.

Adaptive-Loop Design Considerations

The control and regulation functions are performed by the parent PRM in the array. In general, the design procedures for Adaptive-Loop compensation will hold (refer to the product data sheet for the latest design procedure and equations), but some of the parameters must be scaled against the number of PRMs and VTMs in the array, and some parameters may require adjustments.

The Adaptive-Loop engine measures the output current of the parent PRM and the internal temperature of the VTM™. It uses those measurements to compensate for changing load current and temperature. The compensation slope is the negative resistance R_{LL_AL}.

From the PRM data sheet, to determine the value of the compensation slope R_{LL_AL}, it is helpful to reflect the VTM output resistance to the input of the VTM. Recall that the resistance on the output side of the VTM is scaled by the VTM transformer ratio (K_{VTM}) squared. For parallel VTMs, the reflected resistances of the VTMs are in parallel. V_{OUT} is effectively unchanged from the single VTM case, but I_{OUT} is multiplied by the number of VTMs. If the number of VTMs is N_{VTMs}, the output resistance is reduced by a factor of N_{VTMs}. For parallel VTMs, the equation for the reflected output resistance becomes:

$$R_{OUT\_REFL} = \left(\frac{R_{OUT\_VTM\_25C}}{N_{VTMs}}\right)\frac{1}{(K_{VTM})^2} \qquad (1)$$

Where:

$R_{OUT\_VTM\_25C}$ is the VTM™ output resistance at 25°C

K_{VTM} is the VTM ratio V_{OUT} / V_{IN}

N_{VTMs} is the number of VTMs

For N$_{PRMs}$ parallel PRMs, the output current of each PRM™ must be reduced by N$_{PRMs}$, meaning the reflected resistance is increased by a factor of N$_{PRMs}$. The resulting PRM compensation slope is:

$$R_{LL\_AL} = N_{PRMs} \bullet R_{OUT\_REFL} = N_{PRMs} \bullet \frac{R_{OUT\_VTM\_25C}}{N_{VTMS} \bullet K^2_{VTM}} \qquad (2)$$

Recall from the PRM data sheet that R$_{LL\_AL}$ is set by V$_{AL}$, the voltage difference between the AL pin and SGND pin. For the full-chip and half-chip PRM, use the following formula:

$$R_{LL\_AL} = V_{AL} \bullet G_{AL} \qquad\qquad (3)$$

Where V$_{AL}$ is the voltage on the AL pin and G$_{AL}$ is the AL gain. AL gain is specific to PRM and is specified in the respective PRM data sheet. See the PRM data sheet for more information on setting V$_{AL}$.

Adaptive-Loop operation allows temperature compensation using the output voltage of the VTM's TM pin. (See the PRM data sheet for more details.) In Figure 1, only the TM pin of the parent VTM was used to drive the VT pin of the parent PRM. Figure 2 shows a circuit that improves on this by averaging the output of the TM pins for all VTMs in the array. The summing amplifier prevents impedance mismatches from affecting the compensation loop. In this circuit, the VAUX pin of the parent PRM powers the op-amp; this minimizes the amount of external circuitry required, but care must be taken not to exceed the maximum current and bypass capacitance of the VAUX pin.

***Figure 2**
Temperature Feedback Circuit
for an Adaptive-Loop Array
Using a Summing Amplifier to
Average the TM Signals*
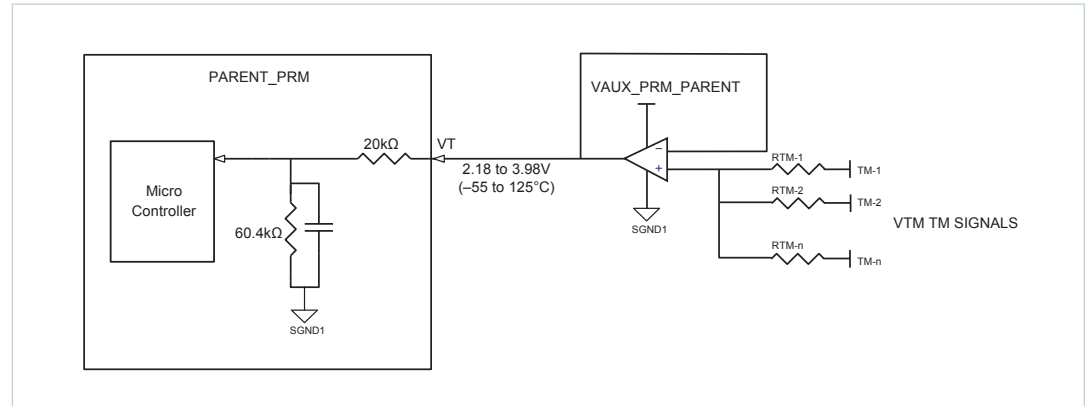
SHARE Pin Limitations

In Adaptive-Loop operation, the limitation of the number of parallel PRMs comes from the limited drive current of the SHARE pin (Figure 3). The SHARE pin of the PRM™ connects to a bidirectional buffer. The voltage on the controller side of the buffer determines the timing of the power train (and ultimately the power delivered to the load). When designated as a parent, an internal error amplifier generates the control signal and the buffer is configured as an output which drives the SHARE bus. In child mode, the internal error amplifier is disabled and the buffer is configured as an input which sinks a small amount of current. In the worst case, the childs draws the share current and the parent SHARE pin is limited to how many childs it can drive. The data sheet states that one parent can drive four childs. So the maximum number of childs would be four; five or more childs would exceed the drive capacity of the parent SHARE pin.

Both the SHARE output buffer of the parent and the SHARE input buffers of the childs have finite resistances which generate an offset between the internal control node of the parent and sense nodes in the childs; the offset current increases as more current is sourced from the SHARE pin. This offset causes timing differences and results in an imbalance in sharing between parent and child devices. The offset current difference is shown as a percentage by the %Difference_Max line in Figure 4. This is the current-share accuracy: lowering the difference means there is a lower imbalance. The benefit of minimizing this value is the increase in array output power deliver to the load.

These limitations can be overcome using external op-amps to buffer the SHARE pin. In Adaptive-Loop operation, the buffers limit the loading on the Parent PRM SHARE pin and prevent the parent PRM from going into current limit prematurely and improve the current sharing among PRMs by minimizing the voltage drops across the series resistance introduced by the internal bidirectional buffer.

Figure 3
SHARE Pin Equivalent Circuit,
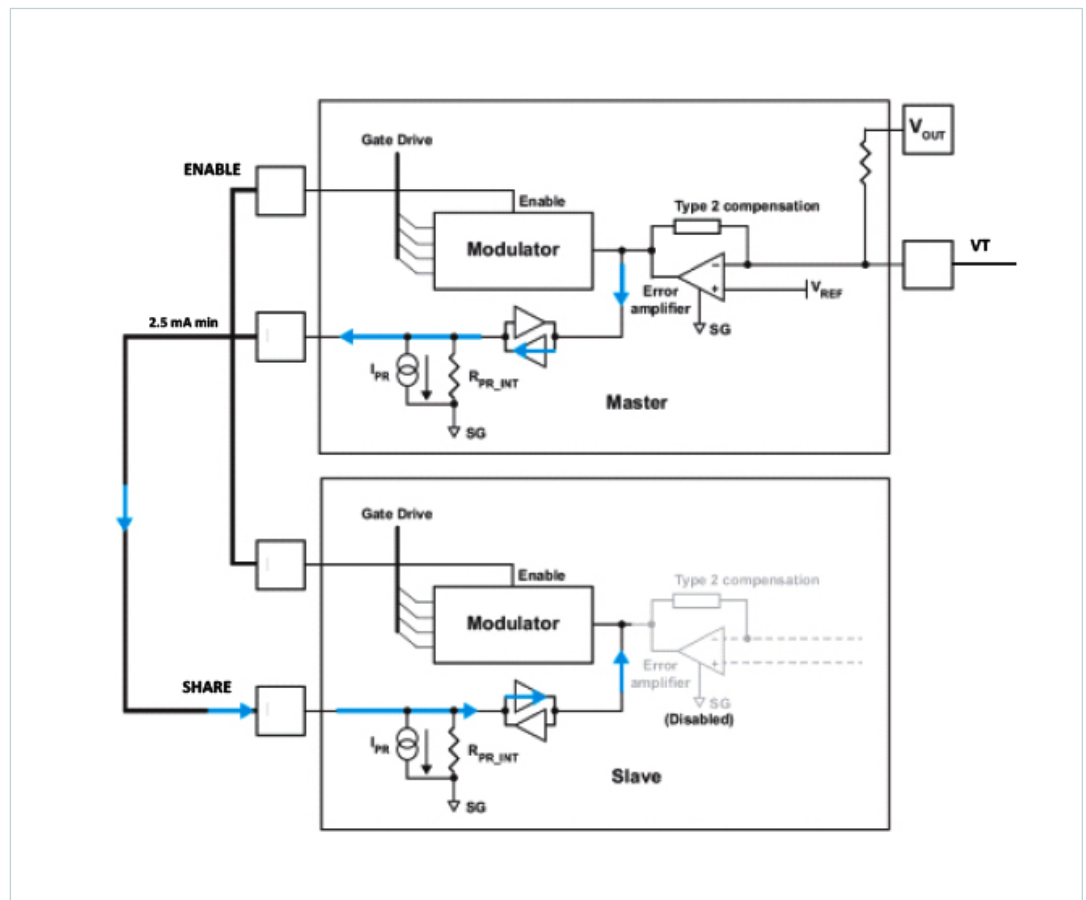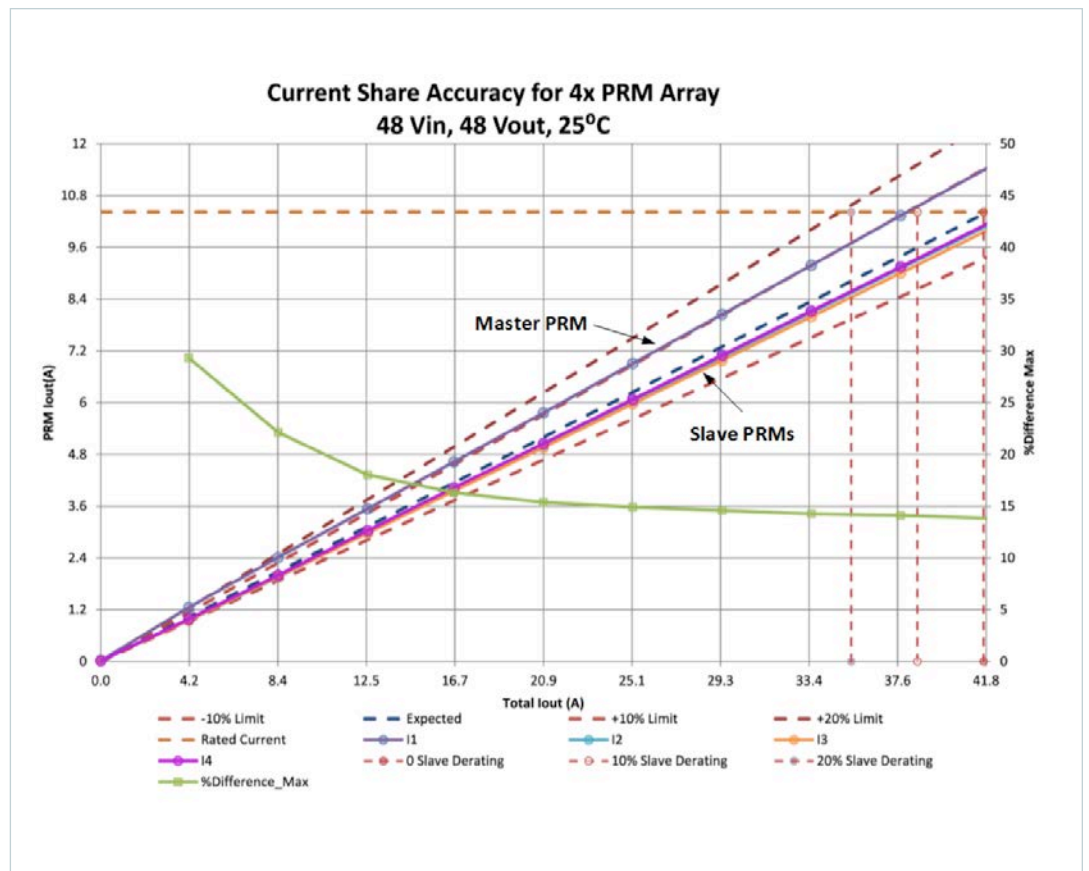*Showing the Source of*
Parent-Child Offset Current

Current Share Accuracy for 4x PRM Array
48 Vin, 48 Vout, 25°C

Arrays of Six or More PRMs (Adaptive-Loop Operation)

For large arrays, external buffers can be added increasing the drive capability of the SHARE bus. The buffers also decrease the load on the parent SHARE pin, reducing the offset between the parent and childs. When using VAUX to power the buffers, the external capacitance limit and current drive capability of VAUX (as specified in PRM™ data sheet) should not be exceeded. The input and output currents of the SHARE pins (I_{SHARE} and I_{SHARE_SINK}, respectively) can be determined from the PRM data sheet.
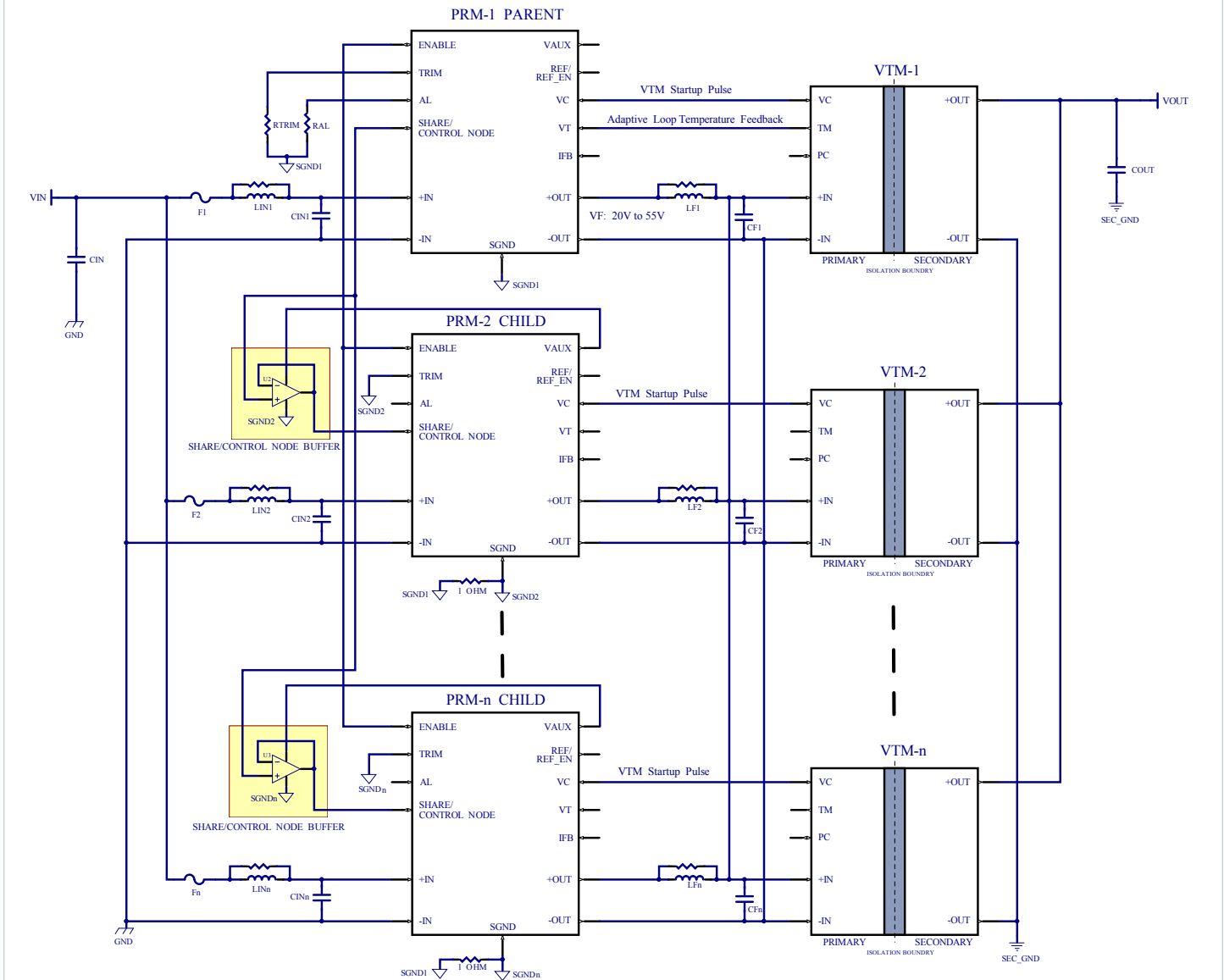

Figure 5
PRM™ – VTM™ Array with SHARE Buffer Circuit

Figure 6 compares the output current of the parent PRM™ to that of the childs. This chart is better because the lower difference means less derating is required for the array. The chart shows the current-share accuracy at or below 10%.

Figure 6

Parent-Child Offset Current of Parallel PRMs with Buffered Share Pin, Showing Reduced Offset
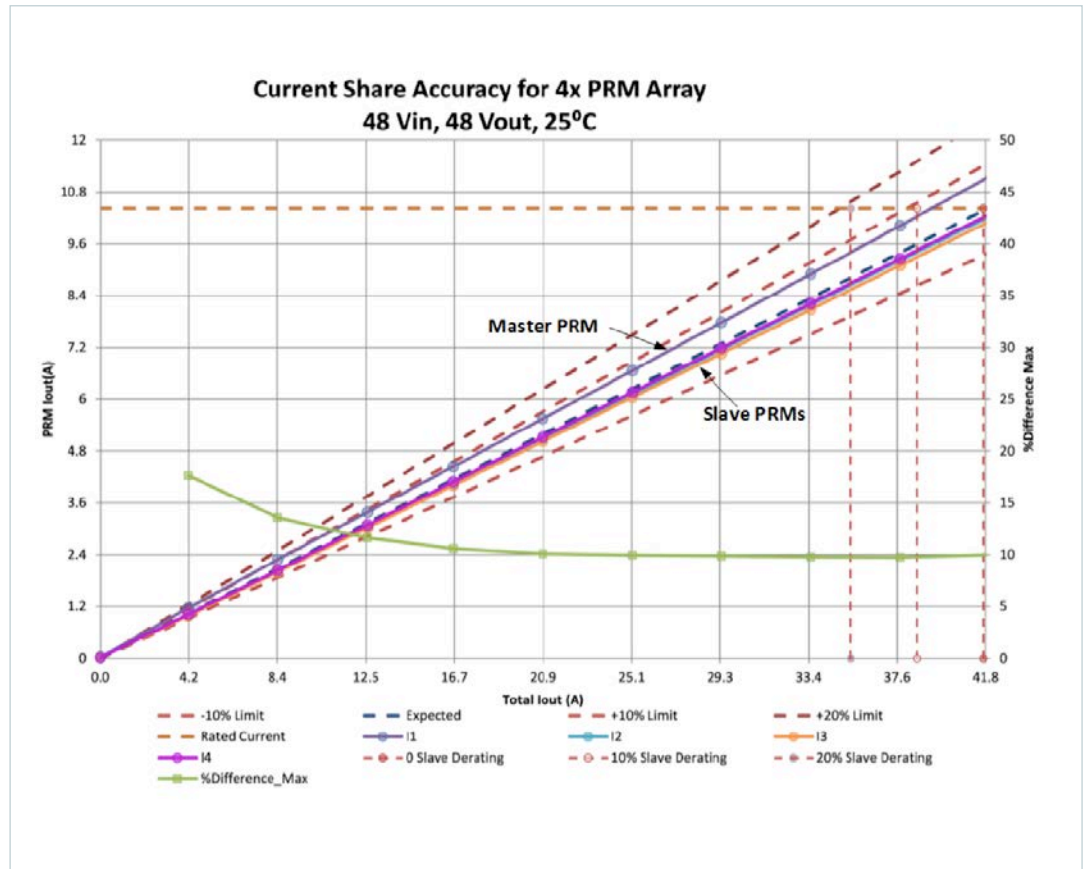
Arrays for Remote-Sense Operation

In Remote-Sense operation, the power capacity of the system can be expanded by placing PRMs in parallel. The number of PRMs that can be placed in parallel depends on the output current of the op-amp that drives the CONTROL NODE pins; for large arrays, the output current of VAUX can be a limitation; in this case, the op-amp can be powered from external circuitry or buffers can be added as explained in a later section. All PRMs within the array are configured for Remote-Sense operation and are driven by an external-control circuit, which uses the control inputs to drive the CONTROL NODE bus.

Figure 7
*PRMs™ and VTMs™
Remote-Sense Array*
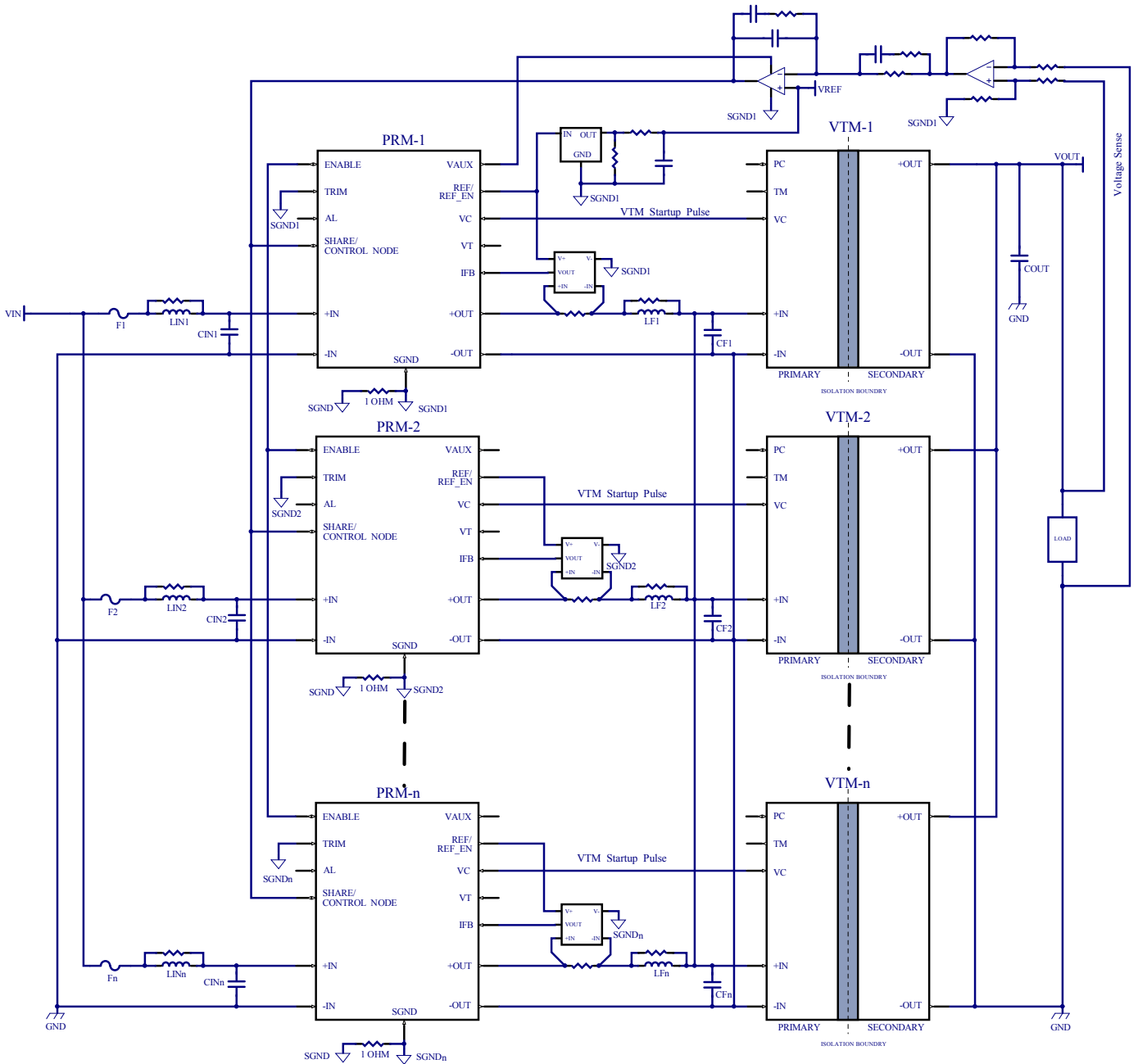
## High-Level Guidelines for Remote-Sense Operation

The following high-level guidelines must be followed in order for the resultant system to start up and operate properly, and to avoid overstress or exceeding any absolute maximum ratings.

- An independent fuse for each PRM +IN connection is required to maintain safety certifications.

- All PRMs™ in the array must be powered from a common power source so that the input voltage to each PRM is the same. The –IN pins of all PRMs must be connected together.

- An independent inductor for each PRM +IN and +OUT connection is required when used in an array to control circulating currents among the PRMs and reduce the impact of beat frequencies.

- ENABLE pins must be connected together for start up synchronization and proper fault response of the array.

- All PRMs must be configured for Remote Sense operation by tying TRIM pins to SGND. Vicor recommends that this connection is made through a 0Ω jumper for troubleshooting purposes.

- Reference supply to the control-loop voltage reference and current-sense circuitry must be powered using R_{EF_EN}.

- A single external control circuit must be implemented as described in the Remote-Sense operation design guidelines. The control circuit should drive the CONTROL NODE bus.

- CONTROL NODE pins must be connected together to enable sharing. The bandwidth requirements of CONTROL NODE are low enough that the bus can be considered a lumped element rather than a transmission line and so star connections as well as daisy-chain connections are permitted.

- Each PRM must have its own local current shunt and current sense circuitry to drive its IFB pin.

- To avoid introducing additional noise, the CONTROL NODE trace length between devices should be minimized and the CONTROL NODE bus should not be routed under any PRM. One PRM should be designated to provide the SGND reference, VAUX and R_{EF_EN} voltages for the external circuitry.

- The SGND pins of all other PRMs should be connected to the SGND reference node on the board through a 1Ω resistor.

- When operating within an array, all the PRMs are derated to the array-rated power and current values provided for Remote-Sense operation (P_{OUT_ARRAY} and I_{OUT_ARRAY} in the PRM data sheet). The number of PRMs required to achieve a given array capacity must take these deratings into account to avoid overstressing the PRMs.

- When using VAUX to power external circuitry, total current draw including CONTROL NODE sink currents must be taken into account. If the maximum VAUX current is exceeded, the external circuitry must be powered from another source.

Control Circuit Design Considerations

Figure 8 shows the small signal model of the PRM™ (see data sheet) with an added load resistance and capacitance represented by R_{LOAD} and C_{OUT_EXT}, which come from the VTM™ input.
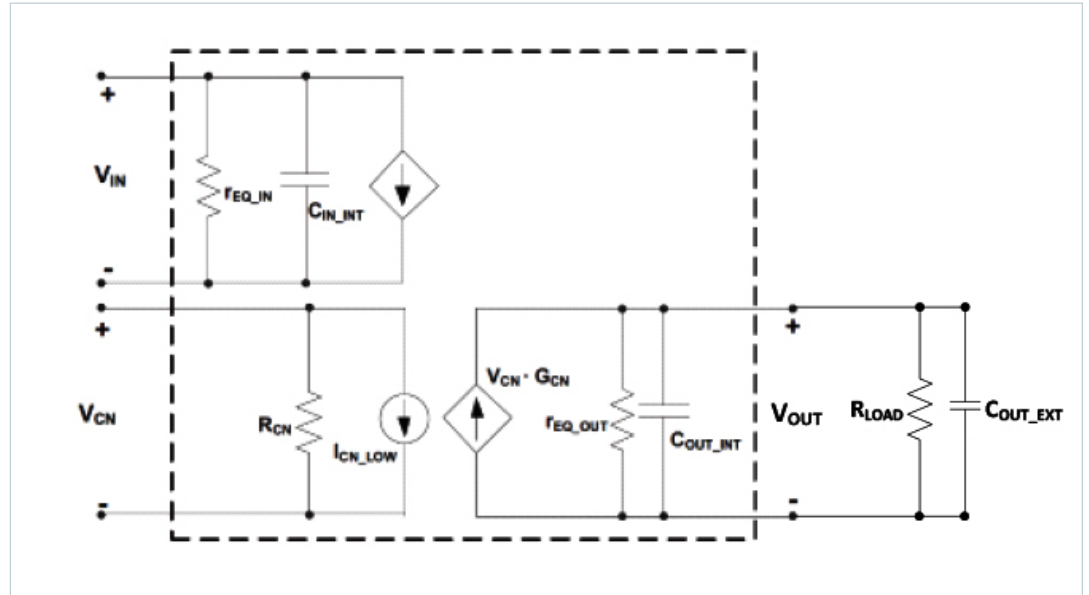
Using the model above, the power train pole and the DC gain for a single PRM are given by the following equations.

Powertrain pole:

$$F_P = \frac{1}{2\pi R_{EQ} C_{EQ}} \qquad (4)$$

Powertrain DC Gain:

$$\frac{V_{OUT}}{V_{CN}} = R_{EQ} G_{CN} \qquad (5)$$

Where:

$$R_{EQ} = \frac{r_{EQ\_OUT} R_{LOAD}}{r_{EQ\_OUT} + R_{LOAD}} \qquad (6)$$

$$C_{EQ} = C_{OUT\_INT} + C_{OUT\_EXT} \qquad (7)$$

For N PRMs™ in parallel, the R_{EQ} term decreases by a factor of N, while the C_{EQ} term and the G_{CN} term increase by a factor of N. This means that the location of the powertrain pole and the value of the powertrain DC Gain are unchanged for N PRMs in parallel. Previous test results also show that compensation that works for one PRM often works for the array as well. It is important to scale and determine the external effective-resistive load value per PRM and effective-capacitance value per PRM. Use the data sheet reference to determine the value of required compensation components.

Limitations on VAUX in Remote-Sense Circuits

The maximum number of parallel PRMs in the power train is due to VAUX output current I_{VAUX} and the error amplifier that drives the CONTROL NODE bus (see Figure 7). Since it is powered by the VAUX pin, the amount of current the error amplifier can source is I_{VAUX} minus the supply current of the op-amp; this current has to be divided up among the PRMs. For example, an LM6142 op-amp driving an array of PRM48Jy480x500A00 PRMs would have 5mA of supply current available from VAUX. The supply current of the LM6142 is 880µA per amplifier; each PRM has a maximum CONTROL NODE Sink Current of 0.75mA. The number of PRMs that could be driven by this circuit is four, since:

$$(5mA - 2(880\mu A)) / 0.75mA = 4.3$$

When specifying bypass capacitors for the amplifier circuit, the powertrain designer must not exceed the maximum capacitance loading of the VAUX pin: 0.04µF in this example.

Figure 9 shows a circuit that avoids these limitations by buffering the CONTROL NODE input of each PRM and powering each buffer with the VAUX pin of the corresponding PRM. In this circuit, the VAUX output doesn't have to supply current for all of the parallel PRMs. In Figure 9, the buffer on PRM-1 reduces loading when many childs are used, but is not required for small arrays since the external circuit could drive the CONTROL NODE of PRM-1 directly. If the error amplifier were to drive the first PRM directly, there might be a difference in the offset current between the first PRM and the others.

The op-amps used for the error amplifier and CONTROL NODE buffering should be wide bandwidth; when powered by VAUX, they should have rail-to-rail inputs and outputs, and be low power. The last two limitations could be eased with an external power source for the amlifiers.

Figure 9
*PRMs™ and VTMs™ in a
Remote-Sense Array with
CONTROL NODE Buffer Circuit*
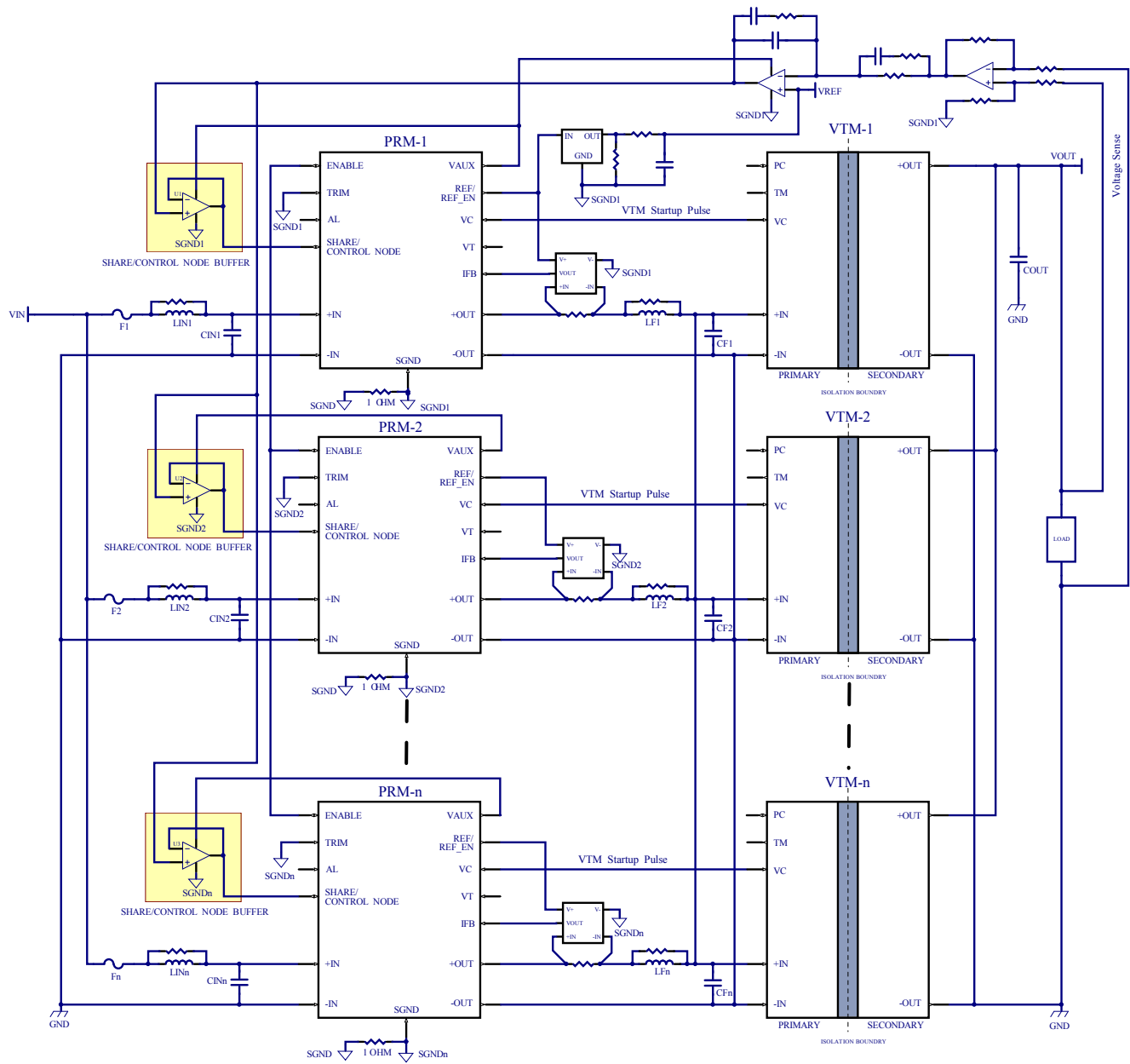
Sizing the Array in Adaptive-Loop and Remote-Sense Operation

Arrays are used to increase the current and power output of the circuit. In the ideal case, the total current from an array of N PRMs™ in parallel would be N times the current of one device. In reality, the current offset between the PRMs causes some difference between the theoretical and the actual output current. The theoretical current must be derated to account for the difference. In Adaptive-Loop arrays, the parent PRM provides the rated current while the childs are derated. For Remote-Sense operation, all PRMs are de-rated.

Using the PRM48Jy480x500A00 in an Adaptive-Loop circuit as an example, Table 1 shows the effect that differential parent-child case temperature has on output current and power. (I_{OUT}, the rated current for a single device is 10.42A.)

Table 1
Effect of Differential Temperature on an Adaptive-Loop Circuit

Attribute	5°C Case Differential	30°C Case Differential
I_{OUT_ARRAY}	8.3A	7.3A
P_{OUT_ARRAY}	400W	350W

Table 2 shows the same PRM48Jy480x500A00, but this time with a Remote-Sense circuit,

Table 2
Effect of Differential Temperature on a Remote-Sense Circuit

Attribute	5°C Case Differential	30°C Case Differential
I_{OUT_ARRAY}	9.4A	8.3A
P_{OUT_ARRAY}	450W	400W

This example above demonstrates that the maximum-output current of an array is obtained with effective temperature management and a Remote-Sense circuit.

The following equations show how the dfference in case temperature is used to calculate the number PRMs required for an array.

Number of PRMs Required for Adaptive-Loop Mode:

For a 5°C case temperature difference, the total number of PRMs required in the array is given by:

$$Total\_PRM\_Array\_I_{OUT} = I_{OUT} + (N_{PRM} - 1) \bullet DRF_A \bullet I_{OUT} \quad (8)$$

Where:

Total_PRM_Array_I_{OUT} is the total PRM array output current

I_{OUT} is the rated output current of one PRM, as specified in the PRM data sheet

N_{PRM} is the number of PRMs required

$DRF_A = I_{OUT\_ARRAY} / I_{OUT}$, the derating factor for this configuration (see Table 1)

This equation can be simplified to calculate the total number of PRM™ required in the array:

$$N_{PRM} = \left[\frac{1}{DRF_A} \left(\frac{Total\_PRM\_Array\_I_{OUT}}{I_{OUT}} - 1 \right) + 1 \right] \quad (9)$$

For a 30 °C case temperature difference, the derating factor goes from DRF$_A$ to DRF$_B$ (see Table 1), so the Equation (9) becomes:

$$N_{PRM} = \left[\frac{1}{DRF_B} \left(\frac{Total\_PRM\_Array\_I_{OUT}}{I_{OUT}} - 1 \right) + 1 \right] \quad (10)$$

Number of PRMs Required for Remote Sense mode:

All PRMs are derated in remote sense operation. For a 5°C case temperature difference in a Remote Sense circuit, the derating factor (I_{OUT_ARRAY} / I_{OUT}) is DRF$_C$ (see Table 2), so the total number of PRMs required in the array is:

$$Total\_PRM\_Array\_I_{OUT} = N_{PRM} \bullet DRF_C \bullet I_{OUT} \quad (11)$$

Where:

Total_PRM_Array_I$_{OUT}$ is the total PRM array output current

I$_{OUT}$ is the rated output current of one PRM, as specified in the PRM data sheet

N$_{PRM}$ is the number of PRMs required

Solving for N$_{PRM}$,

$$N_{PRM} = \left[\frac{1}{DRF_C} \left(\frac{Total\_PRM\_Array\_I_{OUT}}{I_{OUT}} \right) \right] \quad (12)$$

For a 30 °C case temperature difference, the derating factor becomes DRF$_D$ (see Table 2), so Equation (12) becomes:

$$N_{PRM} = \left[\frac{1}{DRF_D} \left(\frac{Total\_PRM\_Array\_I_{OUT}}{I_{OUT}} \right) \right] \quad (13)$$

It is always recommended to use the web-based PowerBench™ Solution Selector tool on the Vicor website (http://www.vicorpower.com/powerbench) to determine the required number of PRMs and VTMs™ in the array and their model numbers.

VTM™ Considerations (Both Adaptive-Loop and Remote-Sense Operation)

VTMs are paralleled simply by connecting the input and outputs together as illustrated in the previous figures. Each VTM requires a VC signal from a PRM in order to start. Vicor recommends connecting one PRM VC to one VTM VC when possible. However, a single PRM VC can also be used to drive up to two VTM VC pins. If this number is exceeded, an external regulator is recommended. The regulator can be enabled with the ENABLE pin of the PRM so that VC is continuously applied when permitted by the VTM. Otherwise, the regulator should be configured to track the VC pin of the parent PRM to coordinate the application and removal of the VC voltage to the VTM.

In both cases, it is critical to take into consideration the slew rate and the current draw requirements of the VTM VC pin, as specified in the device data sheet.

The total output current of the PRM array is K times the total output current of the VTM array, where K is the transformation factor of the VTM at no load. The total output power of the PRM array is the output voltage of the PRM array times the total output current of the PRM array. The output power of the total PRM array can also be calculated from the VTM array output power and the efficiency of the VTM array.

System Considerations

Faults: When a fault is detected on any PRM, either in an Adaptive-Loop or Remote-Sense array, the 5V source of the ENABLE pin of the PRM under fault is turned off which pulls down the ENABLE pin of all PRMs, shutting off their outputs. The output discharge time depends on the load. The output voltage goes to zero if the discharge time is less than the PRM recovery time. The PRM initiates an auto-restart several times per second as long as the fault condition persists. When the fault is cleared, the pull down on ENABLE is removed and the array goes into a soft start.

All VTM faults latch the VTM powertrain off. After a fault, either the input power to the system as a whole must be cycled or the PRMs must be disabled and enabled by way of their bussed ENABLE pins. Vicor recommends that the voltage on the factorized bus be permitted to return to zero before the PRM is re-enabled, otherwise the soft start of the system may be compromised.

Current limit: In an Adaptive-Loop array, the output current limit is detected by the parent PRM. In a Remote-Sense array, Vicor recommends that the output current limit be implemented with external current sense and feedback circuits at the output of each PRM (see Figure 7). Vicor also recommends the use of a high-side current sense IC with rail to rail output.

Layout Considerations

Please reference application note AN:005 FPA Printed Circuit Board Layout Guidelines for a detailed discussion on PCB layout. Application note AN:005 details board layout recommendations using VI Chip® components, with details on good power connections, reducing EMI, shielding of control signals and techniques to reference the control signals to SGND.

Avoid routing control signals directly underneath the PRM™. It is critical that all control signals (except VC) are referenced to SGND for routing, pull down and bypassing purposes. VC may be referenced either to –OUT of the PRM (–IN of the VTM™) or to SGND.

SGND connects internally to –IN and is the reference for all control signals within the device. In most applications, PRMs are mounted to the same PCB and the SGND pins are connected together to form an SGND reference node for the array. Current in the SGND reference node should be minimized. SGND should not be tied to any other ground in the system, including –IN.

In cases where there is significant resistance between each –IN pin and the common supply return, voltage offsets can be generated between the PRM SGND pins which could cause current flow in the SGND node on the board. Care should be taken to minimize these offsets; otherwise series resistors may be needed between each child SGND pin and the SGND node routed on the board to ensure the maximum SGND current is not exceeded. A child SGND resistor of 1Ω might be typical.

Test Results

Figure 10 shows the relative contributions of the parent and child PRMs to the output current. As before, the solid straight lines show the output current of the PRMs and the dotted lines show the rated current of one device, the expected total output current for the array, that current plus and minus 10% and the expected current plus 20%. The green line represents the maximum difference between the output currents, expressed as a percentage and read along the right axis of the graph.

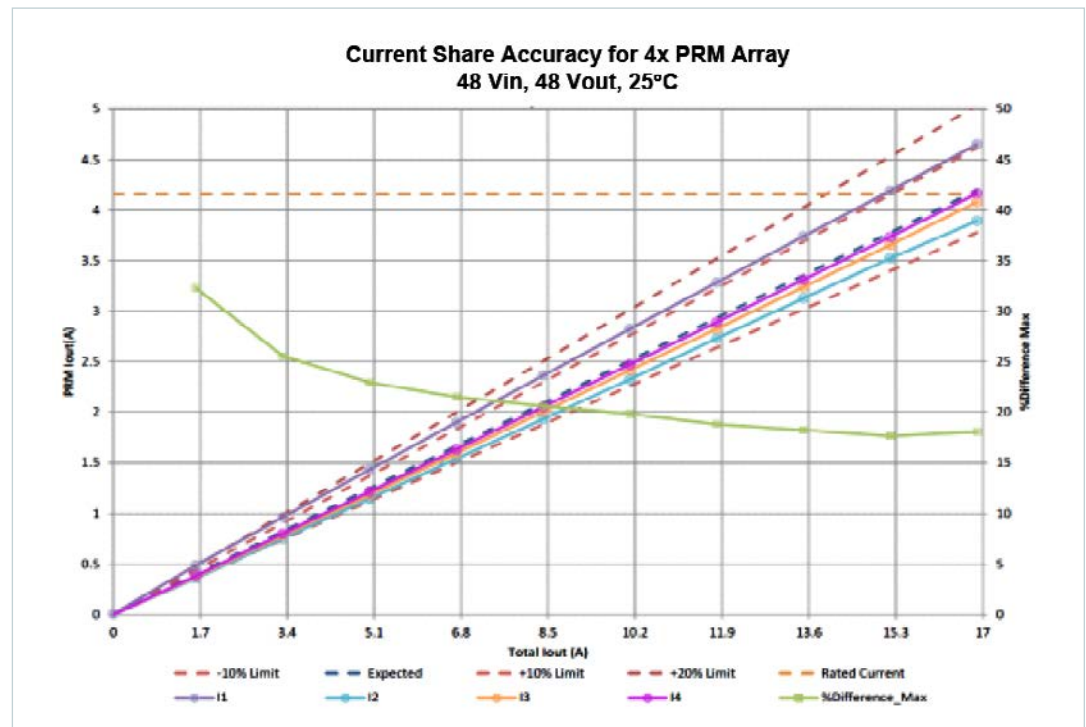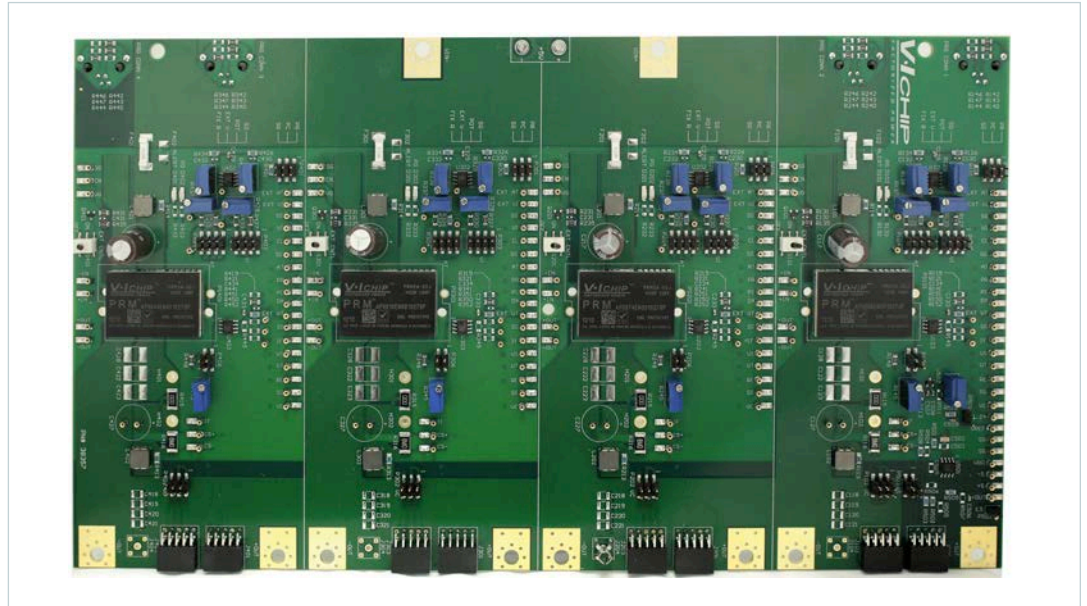*Figure 10*
Current-Share Accuracy
Test Results

Figure 11 shows the board used to evaluate the PRM™ current in the lab.

Figure 11
PRM Evaluation Board

Conclusion

An Adaptive-Loop array is the easiest and most cost-effective way to use the Factorized Power Architecture to generate a high-efficiency power converter. The unique feed-forward architecture allows precise regulation of an isolated PoL voltage without remote sensing and voltage feedback. For optimized performance, the Remote-Sense configuration offers increased flexibility in voltage and current compensation at the cost of a higher component count.

For more information on any of the topics covered in this application note, please contact Vicor Applications Engineering.

Appendix

The following figures show the current-share accuracy for an array of four PRMs in various configurations. Rather than showing an exhaustive list of all possible scenarios, these are intended as a guide to the effects of changing various parameters.

Figure 12
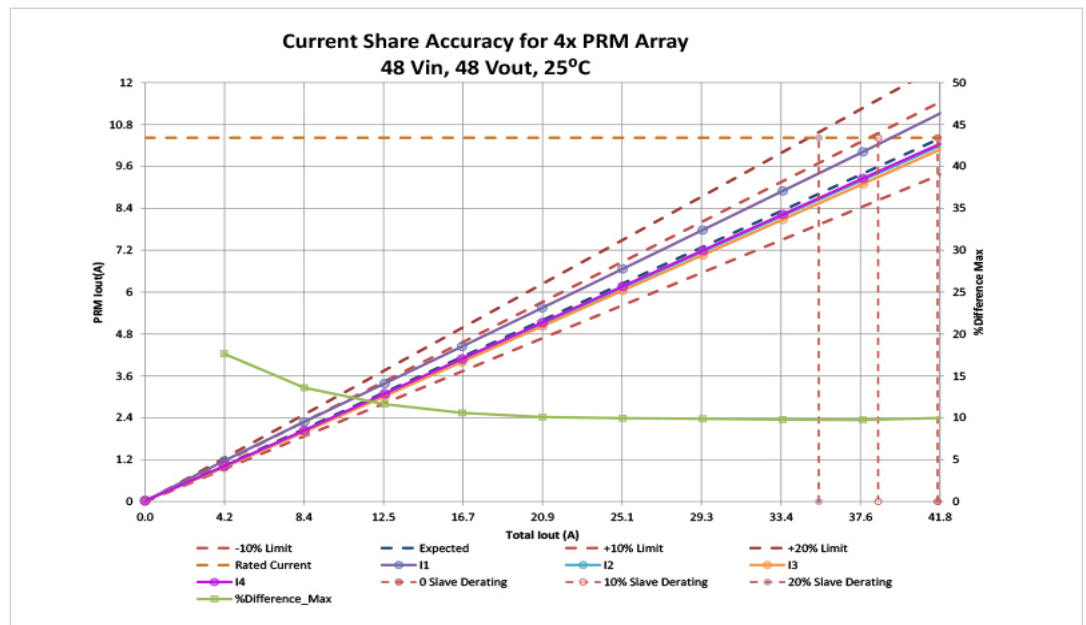*Current-Share Accuracy for Adaptive Loop without Buffer at Room Temperature*
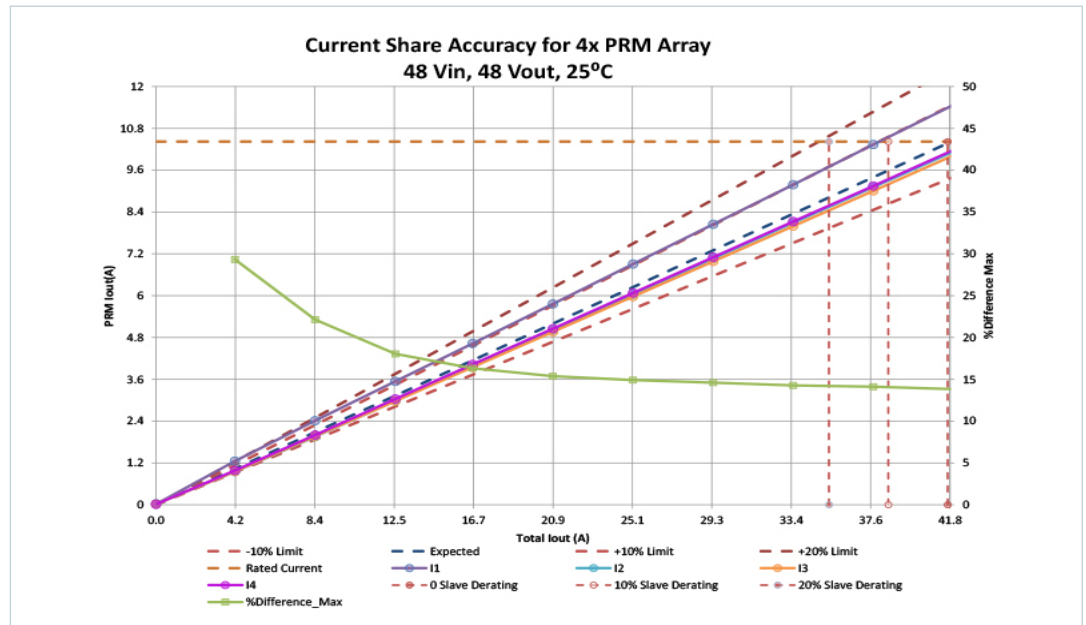
Figure 12 represents Adaptive Loop, 48V input and output, room temperature without a buffer. See Figure 1 for a diagram of the corresponding circuit. The array shown in Figure 1 meets the criteria for 20% derating. The current-share accuracy is adequate for many applications, even though it doesn't meet the 10% design goal.

This plot represents Adaptive Loop, 48V input and output, room temperature with a buffer. See Figure 5 for a diagram of the corresponding circuit.

Figure 13
Current-Share Accuracy for Adaptive Loop with Buffer at Room Temperature

A buffer improves the current-share accuracy to within the 10% design guideline for much of the output-current range. This level of accuracy isn't always required, but can be significant in applications that require a highly-efficient power supply.

Figure 14 shows the Adaptive-Loop circuit without a buffer, 48V input and output, at high temperature.
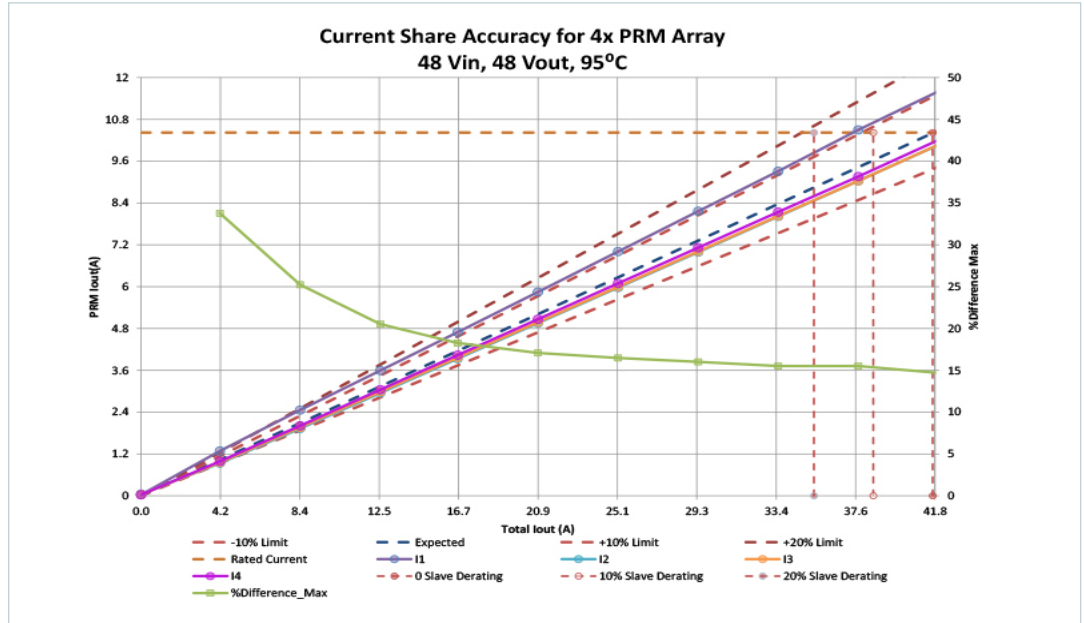
The effect of high temperature is to decrease the efficiency of the power supply by reducing the accuracy of current sharing. The output current still falls within the 20% derating limit for most of the output current range.

This is Adaptive Loop, 48V input and 48V output, at low temperature, without a buffer.
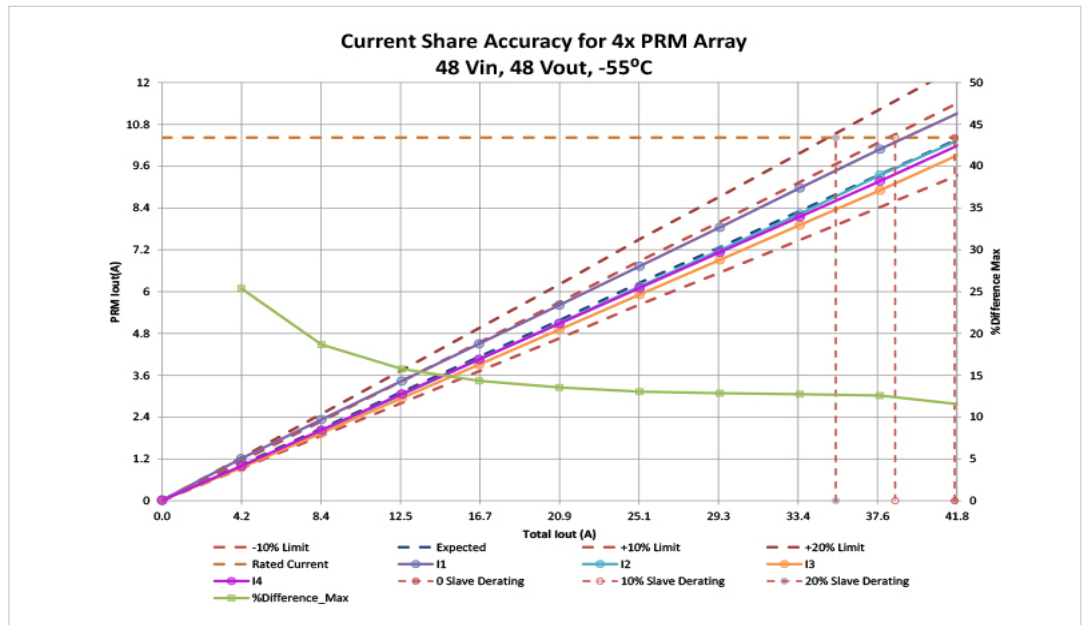
At low temperature, the current-share accuracy is reduced, but to a lesser degree compared to the high-temperature case. Output current is once again within the 10% derating level, except at the lowest levels of output current.

Here are the results for an Adaptive Loop without a buffer, with a high input voltage range and a low output range, at room temperature.
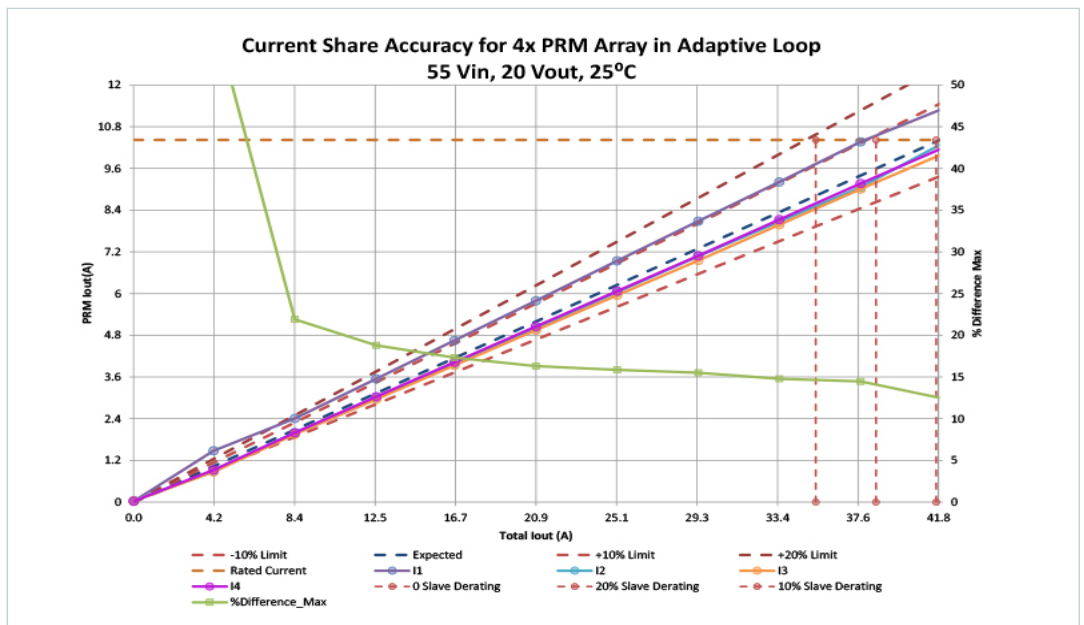
Figure 16

Current-Share Accuracy for Adaptive Loop without Buffer at High V$_{IN}$, low V$_{OUT}$ and Room Temperature
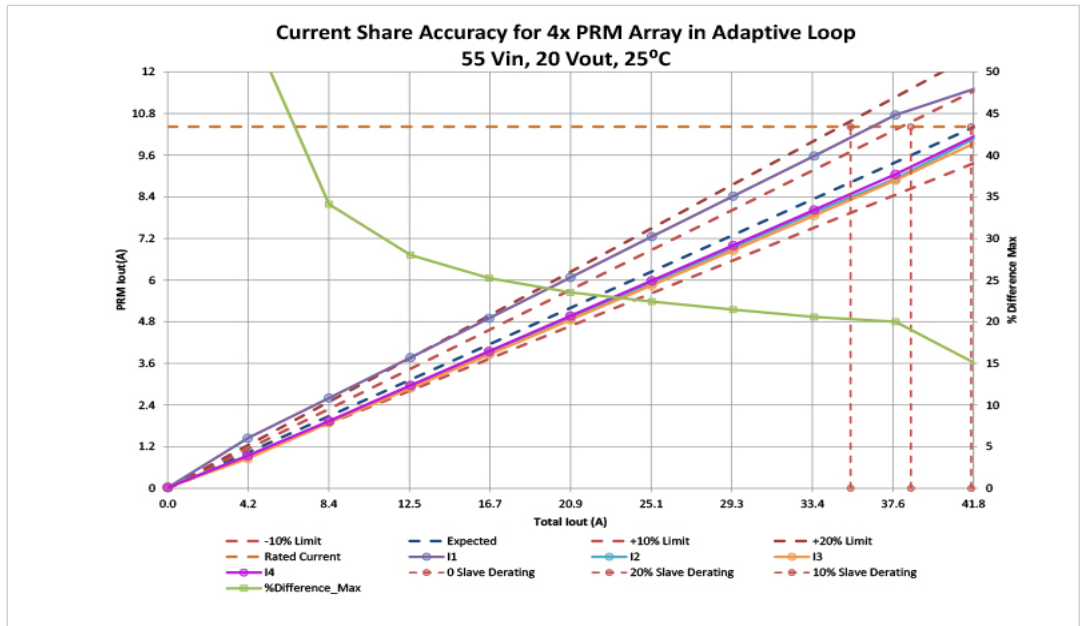
In this case the current-share accuracy is well outside the 10% design goal. This is still an effective circuit for many applications.

Figure 17 shows the Adaptive-Loop circuit under the conditions shown in Figure 16, but this circuit has added buffers.
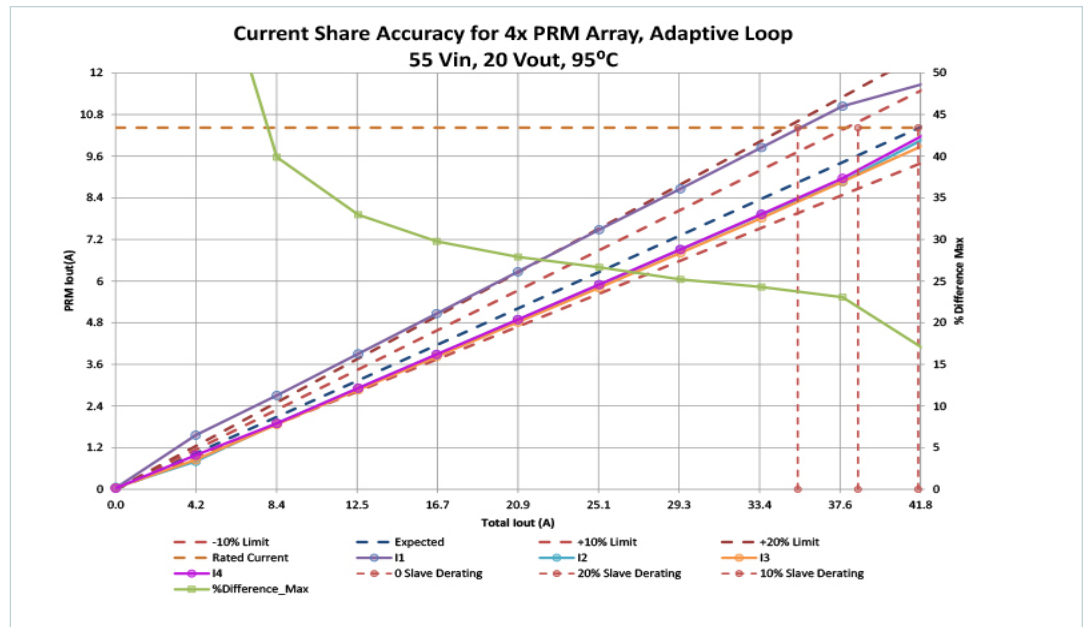
Figure 17

Current-Share Accuracy for Adaptive Loop with Buffer at High V$_{IN}$, low V$_{OUT}$ and Room Temperature

Note how the current-share accuracy is not only improved by the buffers, but the %Difference_Max curve is also much less over a broad range of output currents.

Figure 18 shows the same circuit under the same conditions as above, but at higher ambient temperature.
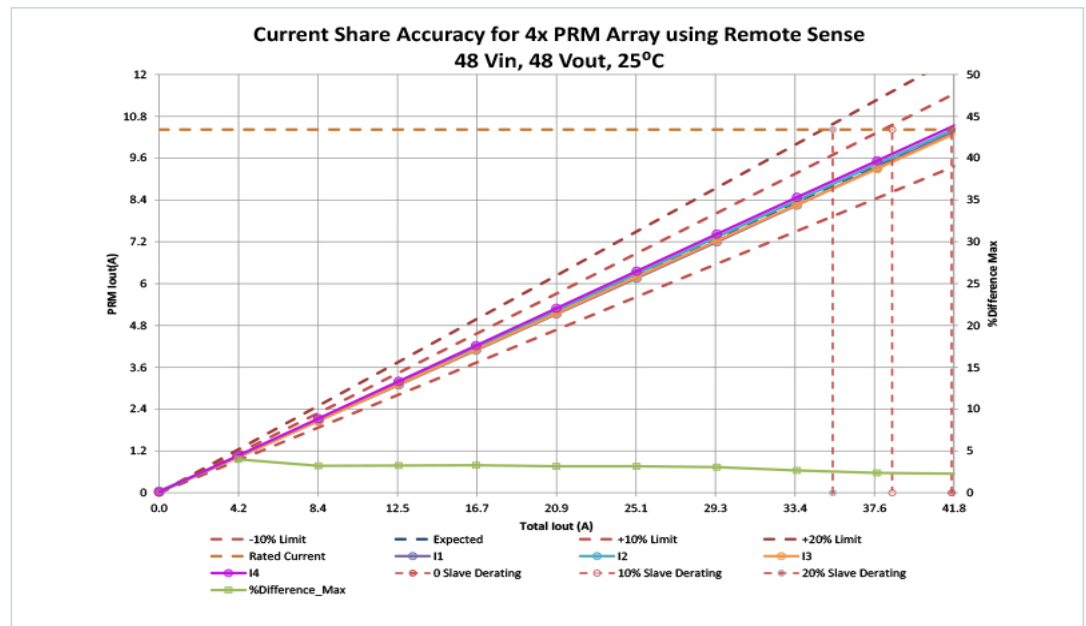
Current Share Accuracy for 4x PRM Array, Adaptive Loop 55 Vin, 20 Vout, 95°C

With no buffer, the effects of high temperature, high input voltage and low output voltage are pronounced.

Figure 19 shows the results for a Remote Sense circuit: 48V input and output, room temperature, with no buffer.
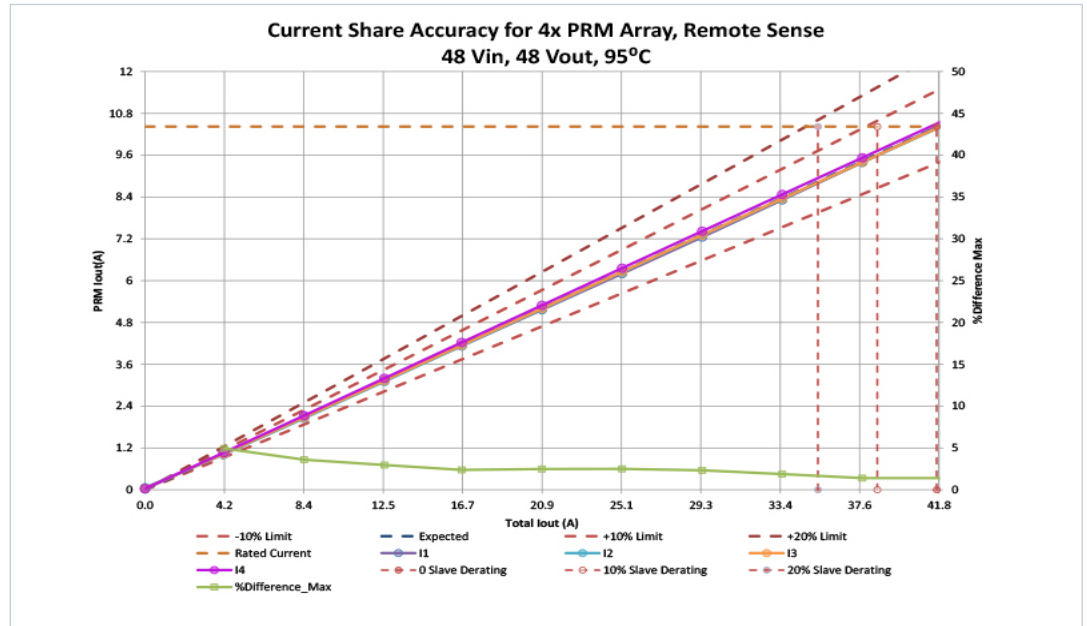
Current Share Accuracy for 4x PRM Array using Remote Sense 48 Vin, 48 Vout, 25°C

Compare this result to that of the Adaptive-Loop array in Figure 12 to see the similarities and differences in the two approaches.

Figure 20 is the result for Remote Sense, high temperature.

The Remote-Sense circuit shows better current-sharing capability than the equivalent Adaptive-Loop circuit due to the lack of offset current in the input and output in the sharing circuit. For a Remote-Sense circuit, the addition of a buffer enables larger arrays but doesn't affect sharing accuracy.

This is Remote Sense at low temperature.
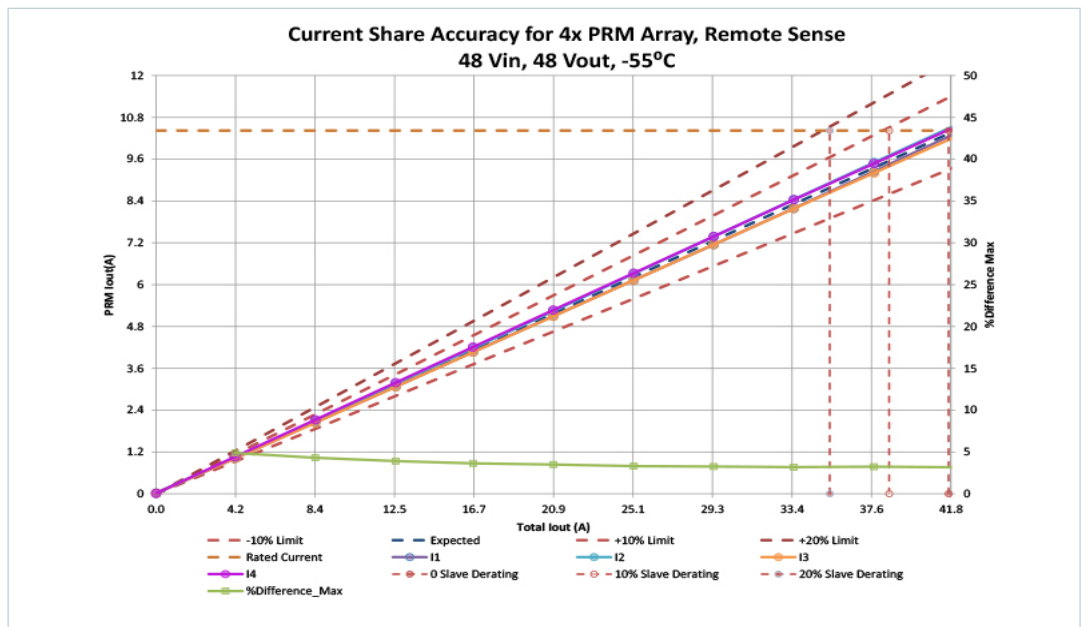
The effects of temperature on current-sharing accuracy in a Remote-Sense circuit are much less pronounced than in the corresponding Adaptive-Loop circuit. There is a relatively small difference in %Difference_Max at low temperature, high temperature (Figure 20) and room temperature (Figure 19) compared to the results for the Adaptive-Loop circuit in Figure 12, Figure 14 and Figure 15.

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