DCM™ in a VIA™ Package DC-DC Converter

DCM5614xD0H36K3yzz

Isolated Regulated DC Converter

Features & Benefits

- Isolated, regulated DC-DC converter
- Up to 1300W, 46.43A continuous
- 96% peak efficiency
- 451W/in^3 power density
- Wide input range 180 – 400V_{DC}
- Safety Extra Low Voltage (SELV) 28V nominal output
- 2121V_{DC} isolation
- ZVS, ZCS high-frequency switching
  - Enables low-profile, high-density filtering
- OV, OC, UV, short circuit and thermal protection
- Fully operational current limit
- Available in chassis-mount and through-hole VIA package
  - 5.57 x 1.40 x 0.37in
    [141.43 x 35.54 x 9.40mm]
- PMBus® management or analog control interface

Typical Applications

- Defense
- Aerospace
- Communications Systems

Product Ratings	
V_{IN} = 270V (180 – 400V)	P_{OUT} = 1300W
V_{OUT} = 28V (22 – 36V) (NO LOAD)	I_{OUT} = 46.43A

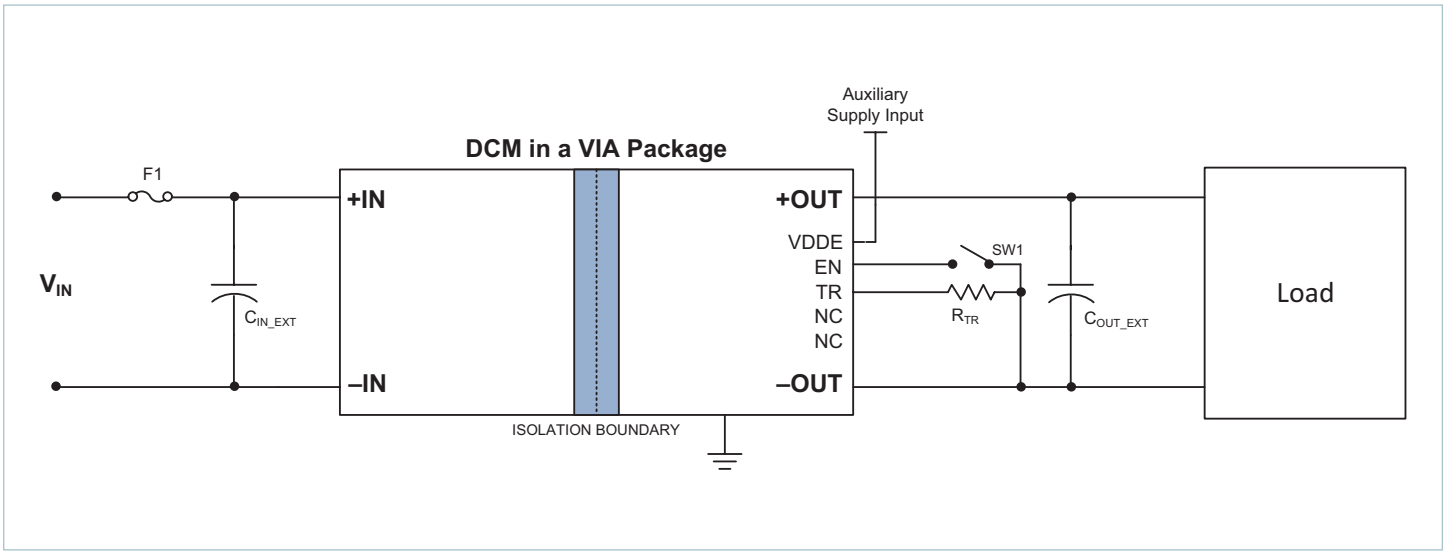
Product Description

The DCM in a VIA package (270 – 28V) is a high-power, high-efficiency DC-DC converter, operating from a 180 – 400V_{DC} primary source to deliver an isolated, regulated, 28V nominal, Safety Extra Low Voltage (SELV) secondary output. This low-profile module, available in chassis- or PCB-mount form-factors, incorporates a DC-DC converter, inrush protection and optional analog or digital communication. The DCM offers low noise, fast transient response and high efficiency and power density. The optional secondary referenced PMBus-compatible telemetry and control interface provides access to the DCM's internal controller configuration, fault monitoring and other telemetry functions. Leveraging the thermal management and power benefits of VIA packaging technology, the DCM module offers flexible mechanical mounting options with low top- and bottom-side thermal resistances. When combined with downstream regulators and PoL current multipliers, the DCM enables power system architects to achieve power-system solutions with outstanding performance metrics and low total cost.

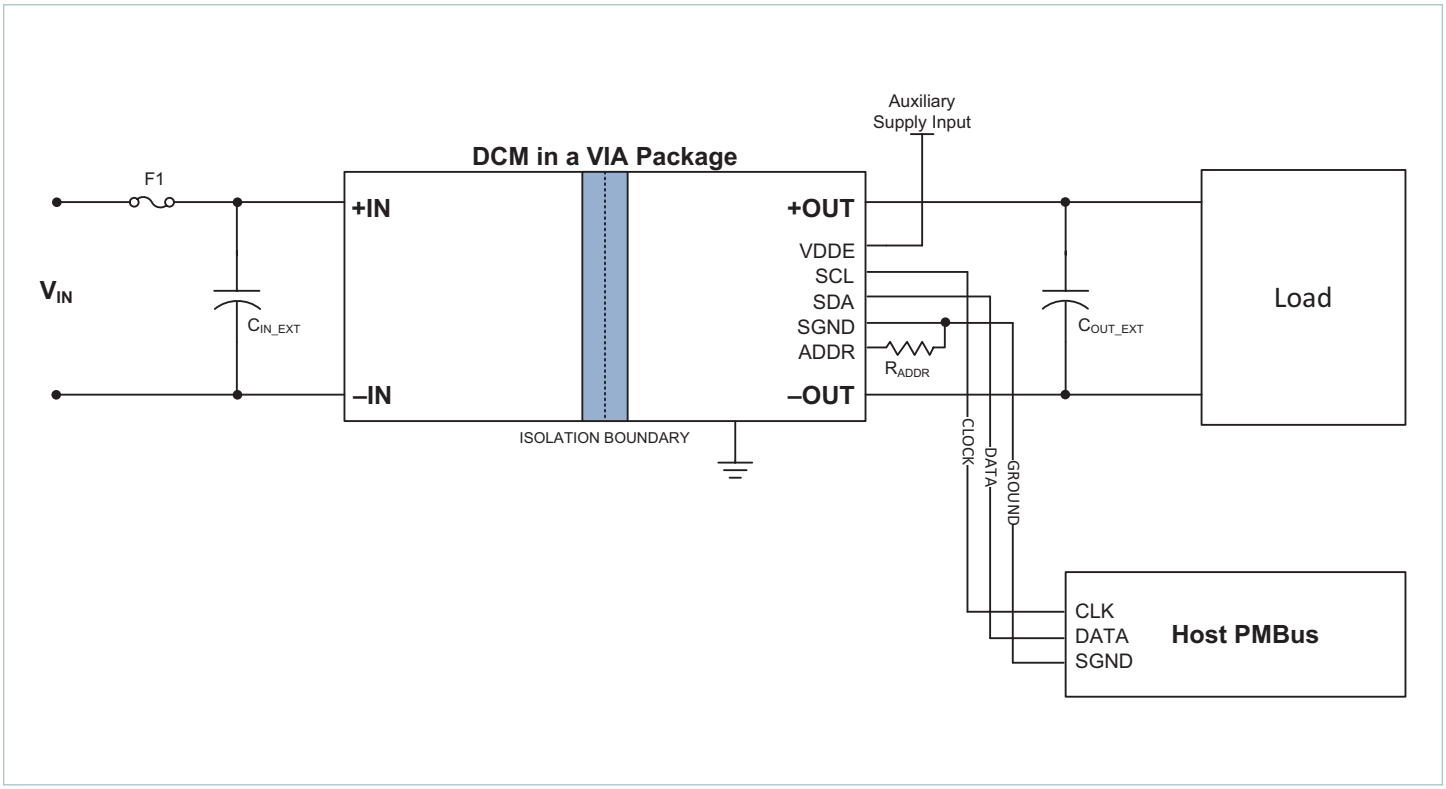
Size:
5.57 x 1.40 x 0.37in
[141.43 x 35.54 x 9.40mm]

Note: Product images may not highlight current product markings and cosmetic features.

Typical Applications

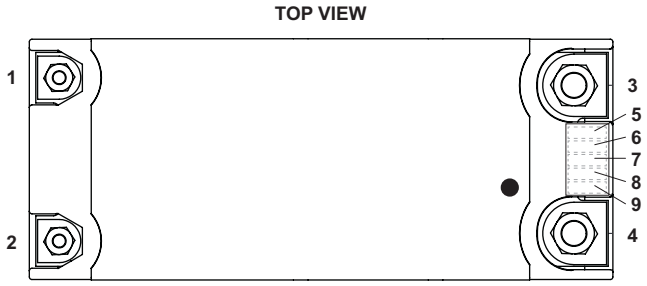


DCM5614xD0H36K3yzz at point-of-load

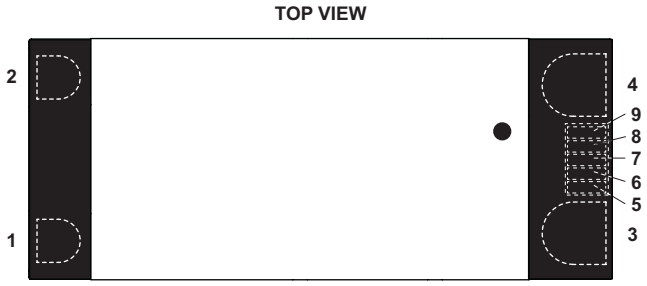


DCM5614xD0H36K3yzz at point-of-load, connection to PMBus®

Pin Configuration



DCM in a VIA package - Chassis Mount



DCM in a VIA package - PCB Mount

Pin Descriptions

Power Pins			
Pin Number	**Signal Name**	**Type**	**Function**
1	+IN	INPUT POWER	Positive input power terminal
2	–IN	INPUT POWER RETURN	Negative input power terminal
3	+OUT	OUTPUT POWER	Positive output power terminal
4	–OUT	OUTPUT POWER RETURN	Negative output power terminal
Analog Control Signal Pins			
Pin Number	**Signal Name**	**Type**	**Function**
5	VDDE	INPUT	External power supply for internal controller
6	EN	INPUT	Enables and disables DCM; needs VDDE pre-applied
7	TR	INPUT	Enables and disables trim functionality, sets the output voltage based on a sampled trim value when trim active
8	NC	–	No connection
9	NC	–	No connection
PMBus® Control Signal Pins			
Pin Number	**Signal Name**	**Type**	**Function**
5	VDDE	INPUT	External power supply for internal controller
6	SCL	INPUT	I^2C Clock, PMBus compatible
7	SDA	INPUT / OUTPUT	I^2C Data, PMBus compatible
8	SGND	LOW-SIDE SIGNAL RETURN	Signal ground
9	ADDR	INPUT	Address assignment, resistor based

Part Ordering Information

Part Number	Package Type	Product Grade	Option Field
DCM5614**V**D0H36K3**T01**	**V** = Chassis VIA	**T** = –40 to 100°C [a]	**01** = Chassis/Analog
DCM5614**V**D0H36K3**T02**			**02** = Chassis/PMBus®
DCM5614**B**D0H36K3**T05**	**B** = Board VIA		**05** = Short Pin/Analog
DCM5614**B**D0H36K3**T06**			**06** = Short Pin/PMBus
DCM5614**B**D0H36K3**T09**			**09** = Long Pin/Analog
DCM5614**B**D0H36K3**TA9**			**A9** = Long Pin/Analog with Dynamic Trim [b]
DCM5614**B**D0H36K3**T10**			**10** = Long Pin/PMBus

[a] High-temperature power de-rating may apply; see Figure 1, specified thermal operating area.
[b] See pin functions and design guidelines specific to this option on pages 21 and 26 – 28.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device. Electrical specifications do not apply when operating beyond rated operating conditions.

Parameter	Comments	Min	Max	Unit
Input Voltage (+IN to –IN)		–0.5	460	V
Input Voltage Slew Rate			1	V/µs
VDDE to SGND		–0.3	12	V
TR to –OUT	Analog interface models only	–0.5	3.6	V
EN to –OUT		–0.5	3.6	V
SCL to SGND	PMBus® interface models only	–0.3	5.5	V
SDA to SGND		–0.3	5.5	V
ADDR to SGND		–0.3	3.6	V
Output Voltage (+OUT to –OUT)			60	V
Dielectric Withstand (Input to Output)	[c] See comment below	2121		V_{DC}
Internal Operating Temperature	T-Grade	–40	125	°C
Storage Temperature	T-Grade	–40	125	°C

[c] The absolute maximum rating listed above for Dielectric withstand (input to output) refers to the VIA package. The internal safety approved isolating component (ChiP™) provides reinforced insulation (4242V) from the input to output. However, the VIA package itself can only be tested at a basic isolation value (2121V).

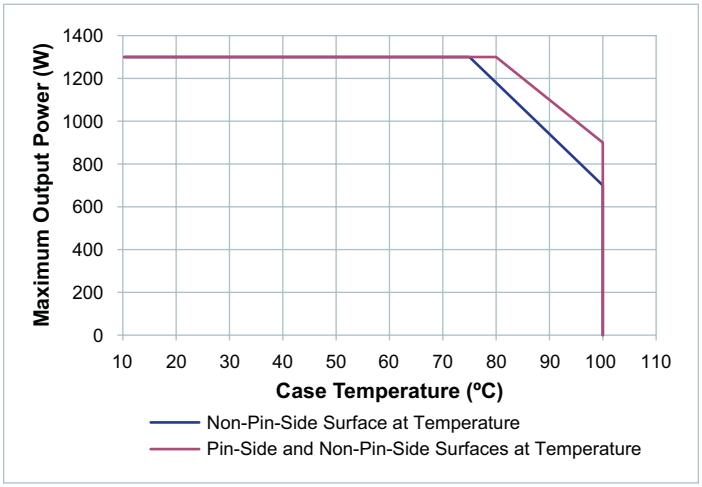


Figure 1 — *Thermal specified operating area: max output power vs. case temp, module at minimum full load efficiency*

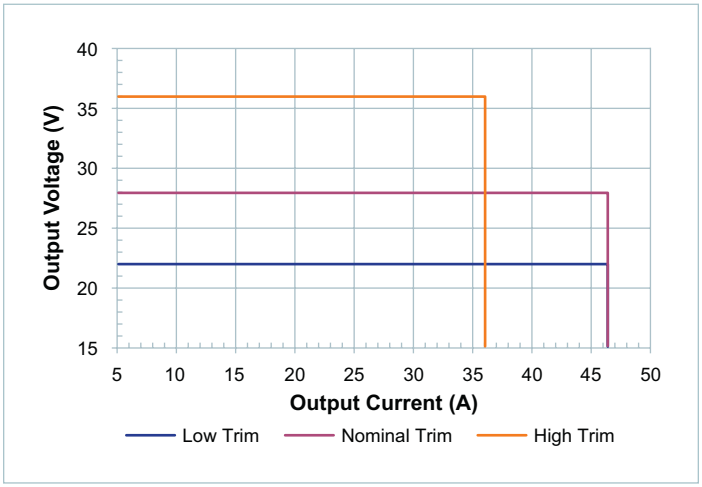


Figure 2 — *Electrical specified operating area*

Electrical Specifications

Specifications apply over all line and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specifications						
Input Voltage Range	V_{IN}	Continuous operation	**180**	270	**400**	V
Inrush Current (Peak)	I_{INRP}	With maximum $C_{OUT-EXT}$, full resistive load			**12**	A
Input Capacitance (Internal)	C_{IN-INT}	Effective value at nominal input voltage		1.2		µF
Input Capacitance (Internal) ESR	$R_{CIN-INT}$	At 1MHz		0.86		mΩ
Input Voltage Initialization Threshold	$V_{IN-INIT}$	Threshold to start t_{INIT} delay			100	V
No-Load Specifications						
Input Power – Disabled	P_Q	Nominal line, see Figure 3		1.6	1.8	W
		Worst case line, see Figure 3			**2.4**	
Input Power – Enabled with No Load	P_{NL}	Nominal line, see Figure 4		13	22	W
		Worst case line, see Figure 4			**27**	

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specifications						
Output Voltage Set Point	$V_{OUT-NOM}$	V_{IN} = 270V, nominal trim, at no load	27.72	28	28.28	V
Rated Output Voltage Trim Range	$V_{OUT-TRIMMING}$	Trim range at no load; Specifies the low, nominal and high trim conditions	**22**	28	**36**	V
Output Voltage Accuracy	$\%V_{OUT-ACCURACY}$	The total output voltage set-point accuracy from the calculated ideal V_{OUT} based on load and trim; Applies over all line, load and trim conditions	**–2**		**2**	%
Rated Output Power	P_{OUT}	Continuous, $V_{OUT} \geq$ 28.0V			**1300**	W
Rated Output Current	I_{OUT}	Continuous, $V_{OUT} \leq$ 28.0V			**46.43**	A
Efficiency	η	Full load, nominal line, nominal trim	92.7	93.7		%
		Full load, over line and temperature, nominal trim	**90.8**			
		50% load, over rated line, temperature and trim	**89.5**			
Output Voltage Ripple	V_{OUT-PP}	V_{IN} = 270V, V_{OUT} = 28V, I_{OUT} = 46.43A, $C_{OUT-EXT}$ = 0µF, 20MHz BW		70		mV
Switching Frequency, Input Stage	F_{RPL-IN}	Nominal line, nominal trim, full rated load, T_{CASE} = 25°C		0.64		MHz
		Over all line, load, trim, exclusive of burst-mode operation	0.3		0.7	
Switching Frequency, Output Stage	$F_{RPL-OUT}$	Over all line, load and trim	0.9	0.95	0.99	
Output Capacitance (Internal)	$C_{OUT-INT}$	Effective value at nominal output voltage		56.7		µF
Output Capacitance (Internal) ESR	$R_{COUT-INT}$	At 1MHz		0.18		mΩ
Rated Output Capacitance (External)	$C_{OUT-EXT}$	All line, 22V ≤ V_{OUT} ≤ 28V, no load; Excessive capacitance may drive module into fault protection; see Figure 16.			**0.75**	F
Equivalent Output Resistance	R_{OUT}	V_{IN} = 270V, nominal trim, at full load, T_{CASE} = –40°C	10	18	28	mΩ
		V_{IN} = 270V, nominal trim, at full load, T_{CASE} = 25°C	12	20	30	
		V_{IN} = 270V, nominal trim, at full load, T_{CASE} = 75°C	12	25	32	
Initialization Delay	t_{INIT}	See state diagram		7		ms
Output Turn-On Delay	t_{ON}	From rising edge EN or acknowledgement of OPERATION command with V_{IN} pre-applied; See timing diagram		25		ms
Output Turn-Off Delay	t_{OFF}	From falling edge EN or acknowledgement of OPERATION command. See timing diagram.			1	ms
Soft-Start Ramp Time	t_{SS}	At full rated resistive load, $C_{OUT-EXT}$ = 0µF		200		ms
		At full rated load and $C_{OUT-EXT}$			**1000**	
Output Current at Start Up	$I_{OUT-START}$	Max load current at start up			**46.43**	A
Monotonic Soft-Start Threshold Voltage	$V_{OUT-MONOTONIC}$	Output voltage rise becomes monotonic with 10% of preload once it crosses $V_{OUT-MONOTONIC}$		4		V
Minimum Required Disabled Duration	$t_{OFF-MIN}$	Refers to the minimum time a module must be in the disabled state before it will attempt to start via EN or OPERATION command	**300**			ms
Minimum Required Disabled Duration for Predictable Restart	$t_{OFF-MONOTONIC}$	Refers to the minimum time a module must be in the disabled state before it is guaranteed to exhibit monotonic soft start and have predictable start-up timing		2.5		s
Voltage Deviation (Transient)	$\%V_{OUT-TRANS}$	No $C_{OUT-EXT}$ (10 ↔ 90% load step), excluding load line		< 6		%
Settling Time	t_{SETTLE}			0.5		ms

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protections						
Input Undervoltage Recovery Threshold	$V_{IN-UVLO+}$			162	**175**	V
Input Undervoltage Lockout Threshold	$V_{IN-UVLO-}$		**146.9**	153.4	**160**	V
Input Overvoltage Lockout Threshold	$V_{IN-OVLO+}$			425	**430**	V
Input Overvoltage Recovery Threshold	$V_{IN-OVLO-}$		**400**	418		V
Minimum Output Voltage for Internal Microcontroller Reset	$V_{OUT-MICRO-RESET}$		**2.3**			V
Output Overvoltage Lockout Threshold	$V_{OUT-OVP+}$			40.26	**41.85**	V
Output Overvoltage Recovery Threshold	$V_{OUT-OVP-}$		**37.75**	39.44		V
Minimum Current Limited V_{OUT}	$V_{OUT-UVP}$			12		V
Overtemperature Shut-Down Threshold	$T_{INT-OTP}$	Internal temperature	**125**			°C
Power Limit	P_{LIM}				**1300**	W
V_{IN} Overvoltage to Cessation of Powertrain Switching	$t_{OVLO-SW}$	Independent of fault logic		2		us
V_{IN} Overvoltage Response Time	t_{OVLO}	Fault logic only		50		ms
V_{IN} Undervoltage Response Time	t_{UVLO}				**400**	us
Short Circuit Response Time	t_{SC}				**400**	us
Fault Recovery Time	t_{FAULT}	Powertrain enabled, operational state	200			ms
Temperature Fault Recovery Time	$t_{OTP-FAULT}$	Powertrain enabled, operational state	400			ms
Overcurrent Recovery Time	$t_{CL-FAULT}$	Powertrain enabled, operational state	300			ms
Output Overcurrent Shut-Down Threshold	I_{OUT-CL}	Of rated I_{OUT} max		119		%
Output Current Limit	$I_{OUT-CLCC}$	Analog interface models. Of rated I_{OUT} max. Fully operational current limit, for nominal trim and below.		105		%
Configurable Output Current Limit Range (PMBus® interface models)	$I_{OUT-CLCC-RANGE}$	PMBus interface models. Fully operational current limit, for nominal trim and below. Current limit set point configurable by PMBus command MFR_CONSTANT_CURRENT (E8h).	0		105	%

Analog Control Signal Characteristics

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.
Please note: for chassis mount models, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated for up to 5 insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

Enable: EN

- The EN pin enables and disables the DCM; when held low, the unit will be disabled.
- The EN pin is activated only if VDDE is pre-applied before V_{IN} is applied. Otherwise, EN is inactive and will be ignored until V_{IN} is removed and reapplied.
- The EN pin is referred to the –OUT of the converter and isolated from the primary side.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Any	EN Enable Threshold	$V_{ENABLE-EN}$				**2.31**	V
		EN Disable Threshold	$V_{ENABLE-DIS}$	Needs VDDE pre-applied	**0.99**			V
		Internally Generated V_{CC}	V_{CC}		**3.23**	3.3	**3.37**	V
		EN Internal Pull-Up Resistance to V_{CC}	$R_{ENABLE-INT}$		**9.9**	10	**10.1**	kΩ

Trim: TR

- The TR pin enables and disables trim functionality when VDDE or V_{IN} is initially applied to the DCM converter. See pin functions and design guidelines sections for more information on TR pin operation.
- If TR is not floating at power up and has a voltage less than TR trim enable threshold, trim is active.
- The TR pin has an internal pull-up to V_{CC} and is referenced to the –OUT pin of the converter.
- $V_{TRIM-RANGE}$ represents the trim pin functional limits only. Module performance is guaranteed within rated output voltage trim range.
- $V_{OUT} = 20 + 20.625 \cdot (V_{TRIM}/V_{CC})$ where V_{TRIM} is the voltage present on the TR pin.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Start Up	TR Trim Disable Threshold	$V_{TRIM-DIS}$	Trim disabled when TR above this threshold at power up			**3.20**	V
		TR Trim Enable Threshold	$V_{TRIM-EN}$	Trim enabled when TR below this threshold	**3.10**			V
Analog Input	Operational with Trim Enabled	Internally Generated V_{CC}	V_{CC}		**3.23**	3.3	**3.37**	V
		TR Pin Functional Range	$V_{TRIM-RANGE}$	Functional limits only	**0**		**2.85**	V
		TR Internal Pull-Up Resistance to V_{CC}	R_{TRIM_INT}		**9.9**	10	**10.1**	kΩ

VDDE

- VDDE powers the internal controller.
- VDDE needs to be pre-applied before V_{IN} in order to activate EN functionalities.
- If not pre-applied, VDDE is derived from V_{OUT}; however, in this case, the enable function is not activated (the unit is always enabled and can be disabled only by removing V_{IN}).

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input	Regular Operation	Power Input for Internal Controller	V_{VDDE}		4	5	10	V
		VDDE Current Consumption	I_{VDDE}			35	50	mA
		Minimum VDDE for Internal Micro-controller Reset	$V_{VDDE-MICRO-RESET}$		0.4			

PMBus® Reported Characteristics

Specifications apply over all line and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range.

Monitored Telemetry					
Attribute	**PMBus Read Command**	**Accuracy (Rated Range)**	**Functional Reporting Range**	**Update Rate**	**Reported Units**
Input Voltage	(88h) READ_VIN	±2% (LL – HL)	130 to 450V	200µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Output Voltage	(8Bh) READ_VOUT	±2% (LL – HL)	12 to 41V	200µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Output Current	(8Ch) READ_IOUT	±20% (10 – 25% of FL) ±5% (25 – 119% of FL)	0 to 55.3A	200µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
Temperature	(8Dh) READ_TEMPERATURE_1	±7°C (Full Range)	–55 to 130°C	400ms	$T_{ACTUAL} = T_{REPORTED}$

Variable Parameters					
• Variables can be written only with $V_{IN} > V_{IN\_UVLO+}$					
Attribute	**PMBus Command**	**Conditions / Notes**	**Accuracy (Rated Range)**	**Functional Reporting Range**	**Default Value**
Output Voltage Trim	(21h) VOUT_COMMAND		±2% (Full Range)	22 – 36V	28V
Constant-Current Threshold	(E8h) MFR_CONSTANT_CURRENT	Applied values greater than 105% disable constant current limit operation and command will return a value of 130%	±20% (0 – 25% of FL) ±5% (25 – 105% of FL)	0 – 105% 130%	105%

PMBus® Control Signal Characteristics

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.
Please note: for chassis mount models, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated for up to 5 insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

VDDE

- VDDE powers the internal controller.
- VDDE needs to be pre-applied before V_{IN} in order to activate OPERATION command functionalities
- If not pre-applied, VDDE is derived from V_{OUT}; however, in this case, the OPERATION command function is not activated (the unit is always enabled and can be disabled only by removing V_{IN}).

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input	Any	Power Input for Internal Controller	V_{VDDE}		4	5	10	V
		VDDE Current Consumption	I_{VDDE}			35	50	mA
	Start Up	Turn-On Time	$t_{VDDE-ON}$	From $V_{VDDE-MIN}$ to PMBus active		1.5		ms

Signal Ground: SGND

- All PMBus interface signals (SCL, SDA, ADDR) are referenced to SGND pin.
- SGND pin also serves as return pin (ground pin) for VDDE.
- SGND pin and low-voltage-side power-return terminal (–OUT) are common.
  To avoid noise interference, keep SGND signal separated from –OUT in electrical design.

Serial Address (PMBus Address): ADDR

- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during start up and is stored until power is reset. This pin programs only a fixed and persistent address.
- This pin has an internal 10kΩ pull-up resistor to 3.3V V_{CC}.
- 16 addresses are available. The range of each address nominally 206.25mV (total range for all 16 addresses is 0 – 3.3V).

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Multi-Level Input	Regular Operation	ADDR Input Voltage	V_{SADDR}		0		3.3	V
		ADDR Leakage Current	I_{SADDR}	Leakage current			1	µA
	Start Up	ADDR Registration Time	t_{SADDR}	From V_{VDDE_MIN}		1		ms

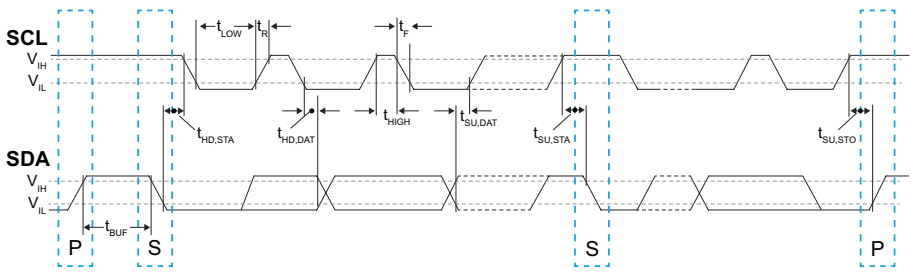
PMBus® Control Signal Characteristics (Cont.)

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.
Please note: for chassis mount models, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated for up to 5 insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

Serial Clock Input (PMBus Clock) and Serial Data (PMBus Data): SCL, SDA

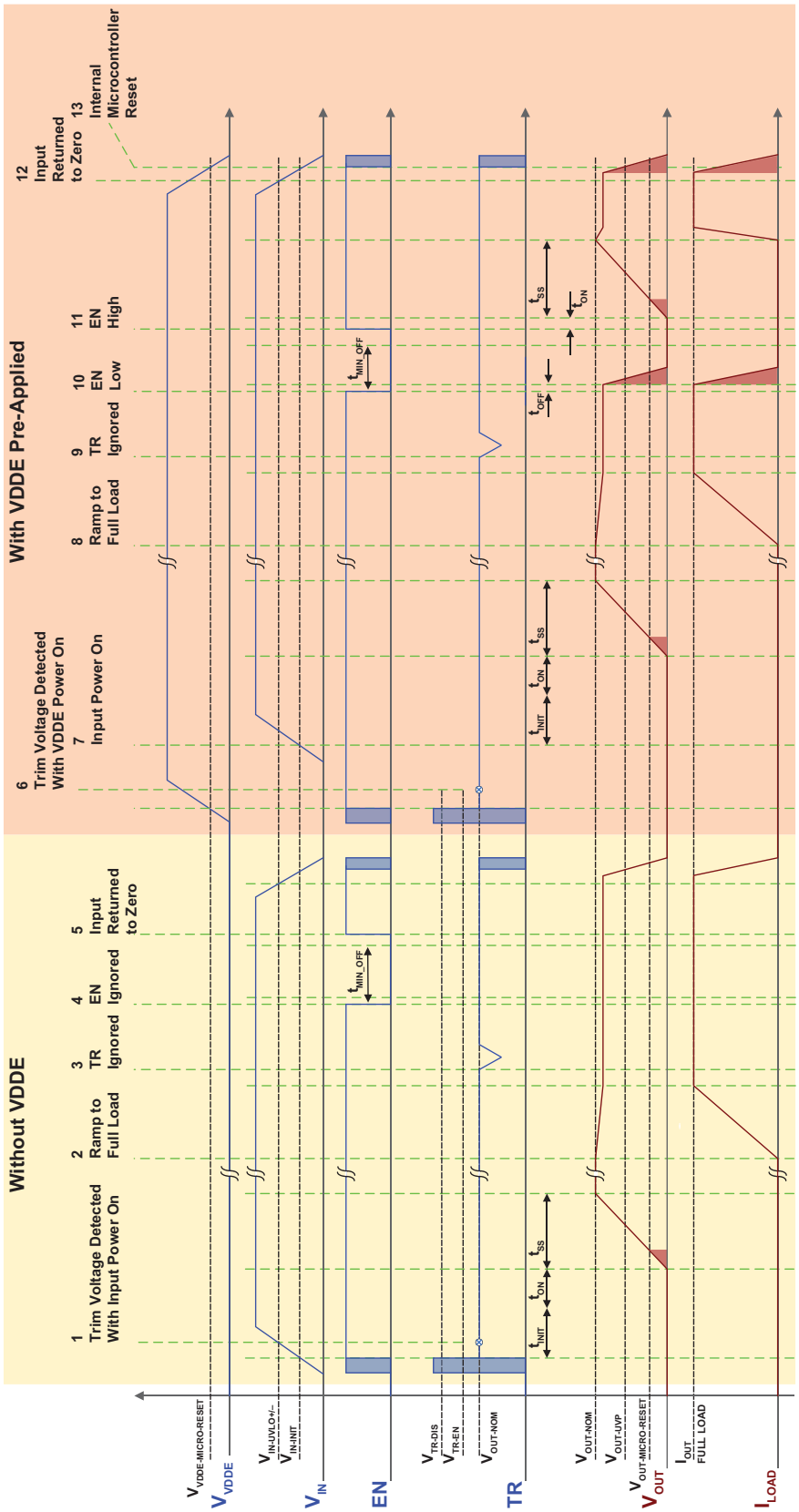
- High-power SMBus specification physical layer compatible. Note that optional SMBALERT# is signal not supported.
- PMBus command compatible.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input / Output	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}		2.3			V
			V_{IL}				1	V
		Output Voltage Threshold	V_{OH}		2.8			V
			V_{OL}				0.5	V
		Leakage Current	$I_{LEAK-PIN}$	Unpowered device	–10		10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one pin			10	pF
		Signal Noise Immunity	$V_{NOISE-PP}$	10 – 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	kHz
		Free Time Between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold Time After Start or Repeated Start Condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Set-Up Time	$t_{SU:STA}$		0.6			µs
		Stop Condition Set-Up Time	$t_{SU:STO}$		0.6			µs
		Data Hold Time	$t_{HD:DAT}$		300			ns
		Data Set-Up Time	$t_{SU:DAT}$		100			ns
		Clock Low Time-Out	$t_{TIMEOUT}$		25		35	ms
		Clock Low Period	t_{LOW}		1.3			µs
		Clock High Period	t_{HIGH}		0.6		50	µs
		Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall Time	t_F		20		300	ns
		Clock or data rise time	t_R		20		300	ns



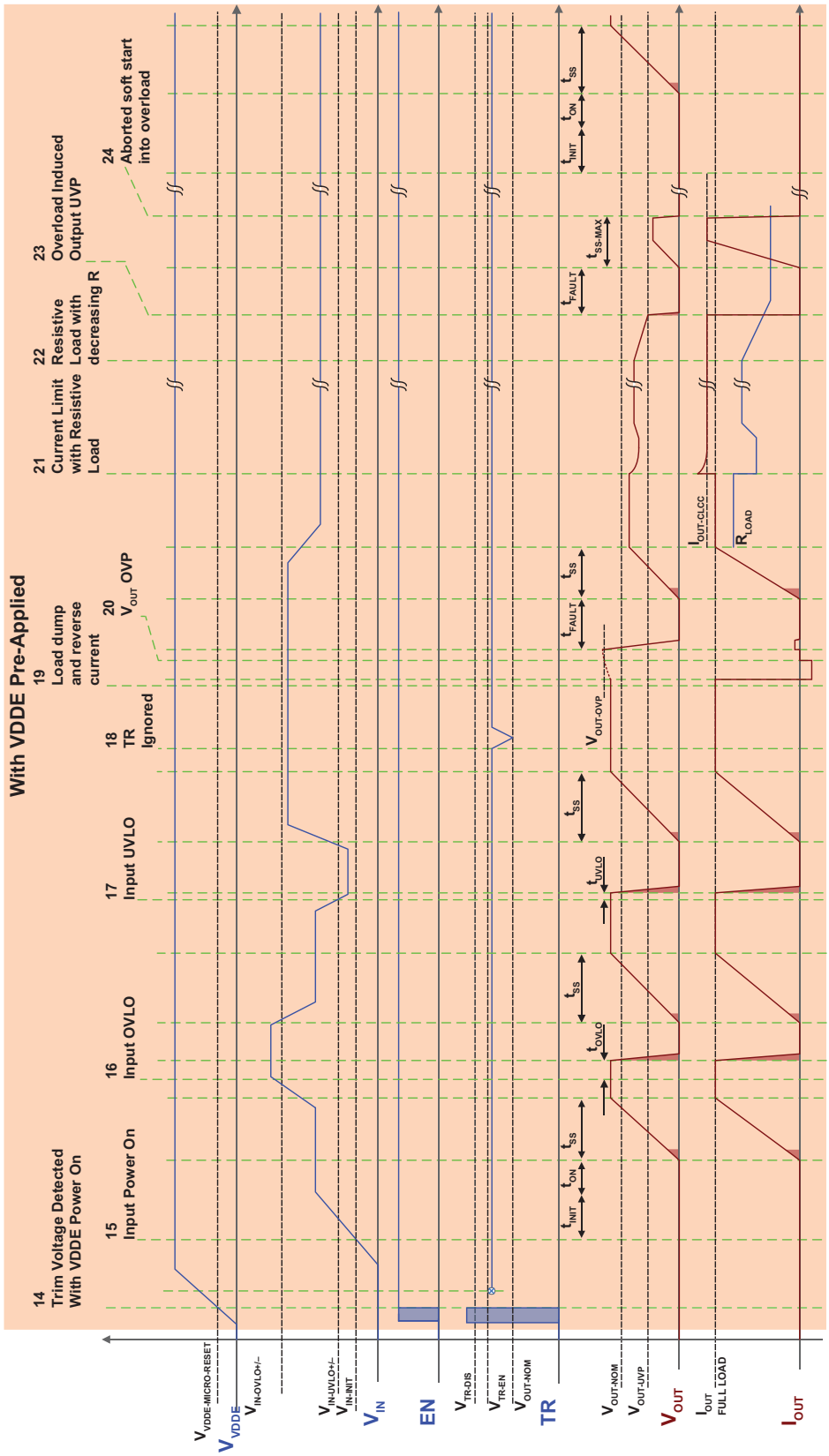
Timing Diagrams – Analog Interface Version

Module inputs are shown in blue; module outputs are shown in brown. Timing diagrams assume VDDE pre-applied. Without VDDE pre-applied, EN is ignored, EN and TR will go high after V_{OUT}. All other behaviors (OVLO, UVLO, OVP, etc.) will remain the same.



Timing Diagrams – Analog Interface Version (Cont.)

Module inputs are shown in blue; module outputs are shown in brown. Timing diagrams assume VDDE pre-applied. Without VDDE pre-applied, EN is ignored, EN and TR will go high after V_{OUT}. All other behaviors (OVLO, UVLO, OVP, etc.) will remain the same.



Application Characteristics

Temperature controlled via non-pin-side cold plate, unless otherwise noted. See associated figures for general trend data.

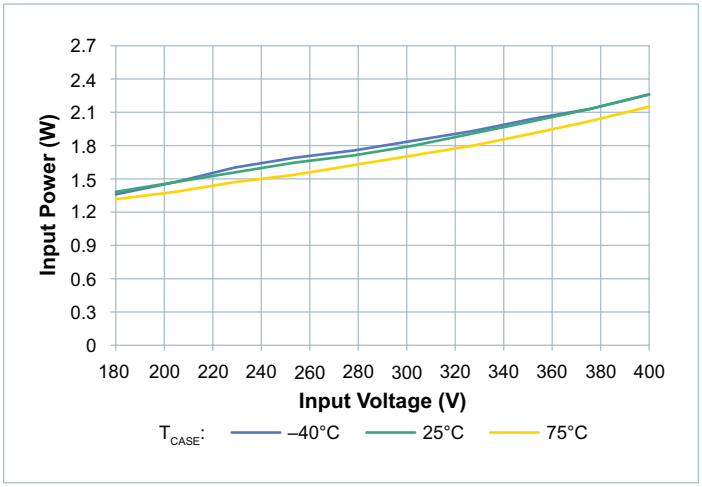


Figure 3 — *Disabled power dissipation vs. V_{IN}*

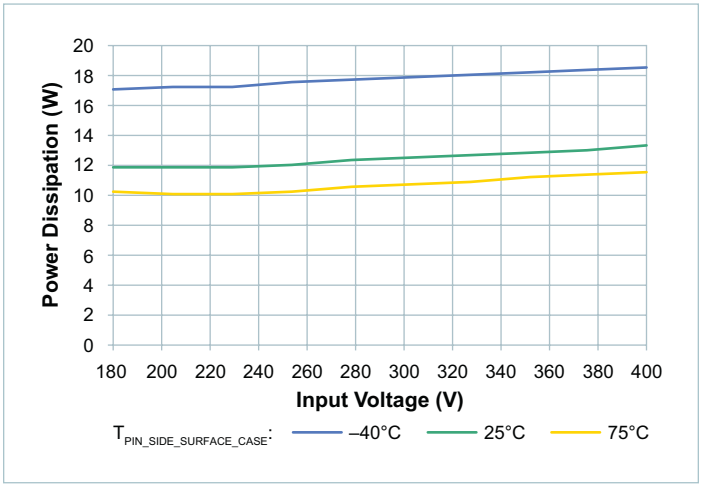


Figure 4 — *No-load power dissipation vs. V_{IN} at nominal trim*

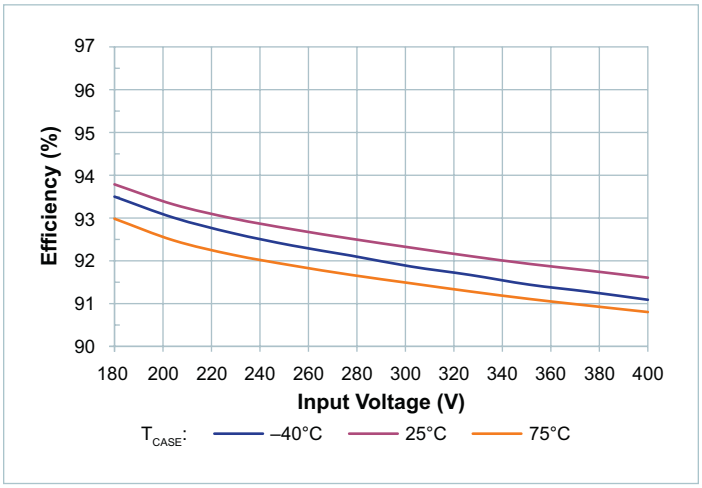


Figure 5 — *Full-load efficiency vs. V_{IN} at low trim*

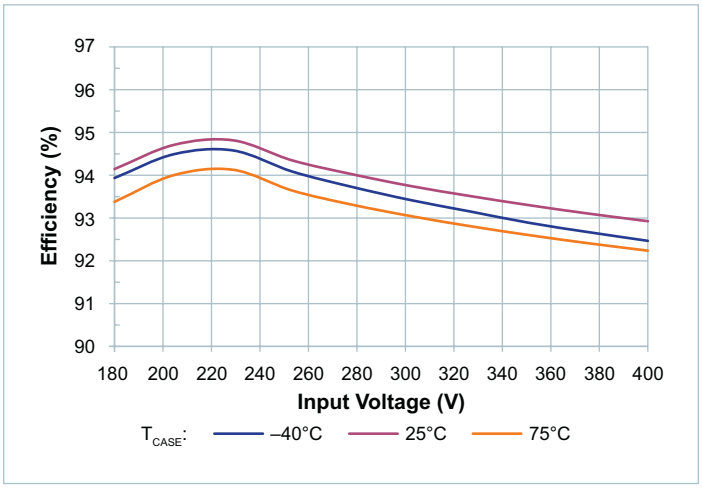


Figure 6 — *Full-load efficiency vs. V_{IN} at nominal trim*

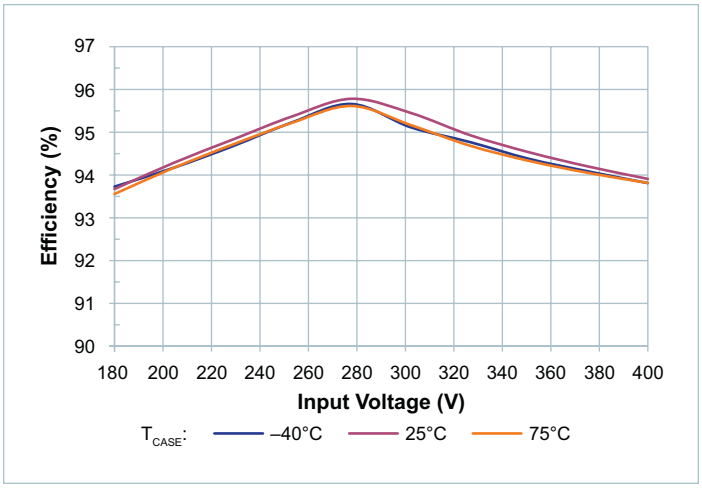


Figure 7 — *Full-load efficiency vs. V_{IN} at high trim*

Application Characteristics (Cont.)

Temperature controlled via non-pin-side cold plate, unless otherwise noted. See associated figures for general trend data.

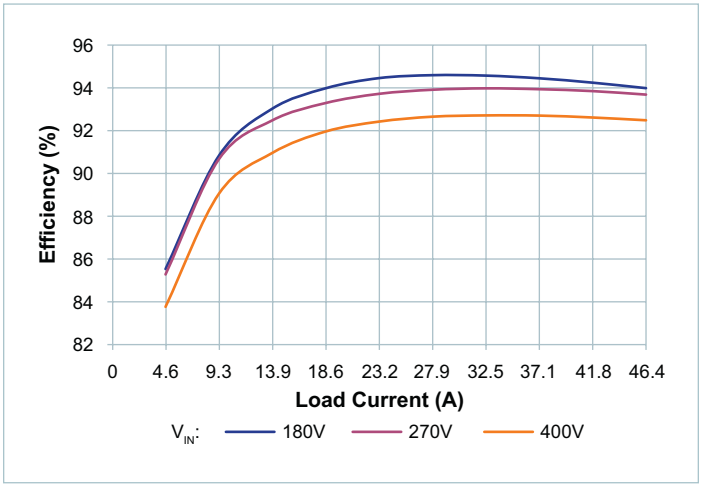


Figure 8 — *Efficiency vs. load at T_{CASE} = –40°C, nominal trim*

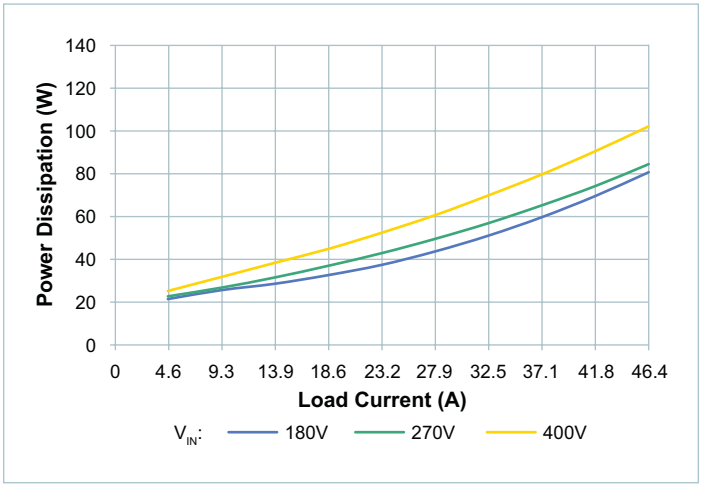


Figure 9 — *Power dissipation vs. load at T_{CASE} = –40°C, nominal trim*

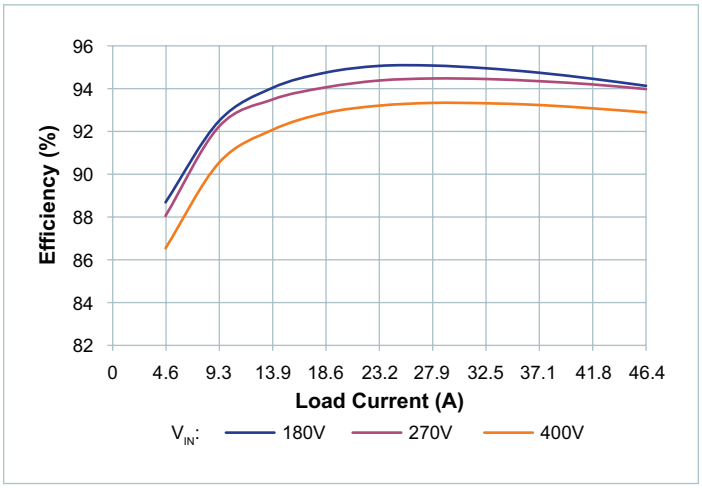


Figure 10 — *Efficiency vs. load at T_{CASE} = 25°C, nominal trim*

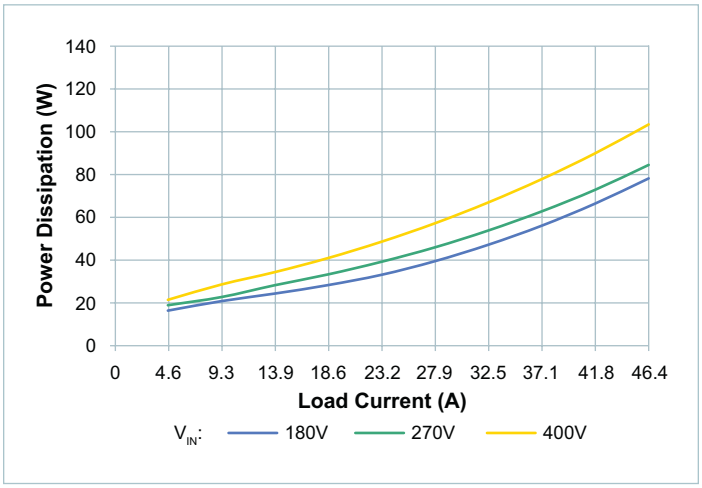


Figure 11 — *Power dissipation vs. load at T_{CASE} = 25°C, nominal trim*

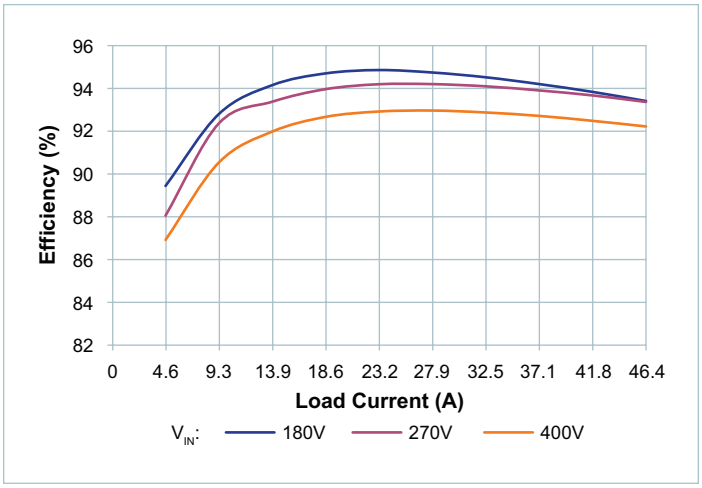


Figure 12 — *Efficiency vs. load at T_{CASE} = 75°C, nominal trim*

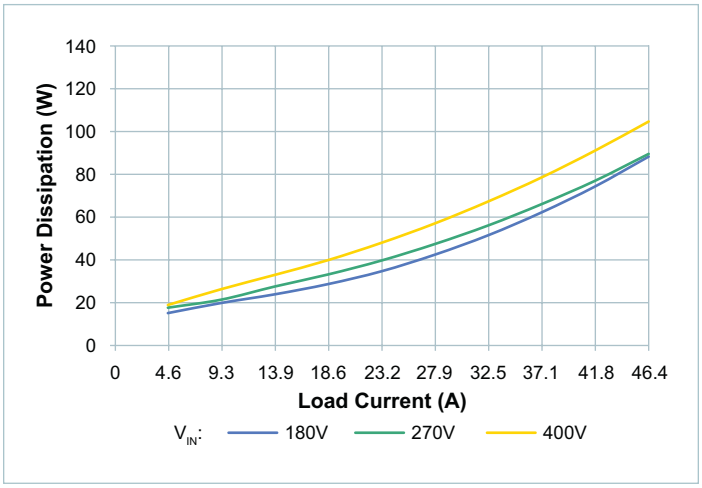


Figure 13 — *Power dissipation vs. load at T_{CASE} = 75°C, nominal trim*

Application Characteristics (Cont.)

Temperature controlled via non-pin-side cold plate, unless otherwise noted. See associated figures for general trend data.

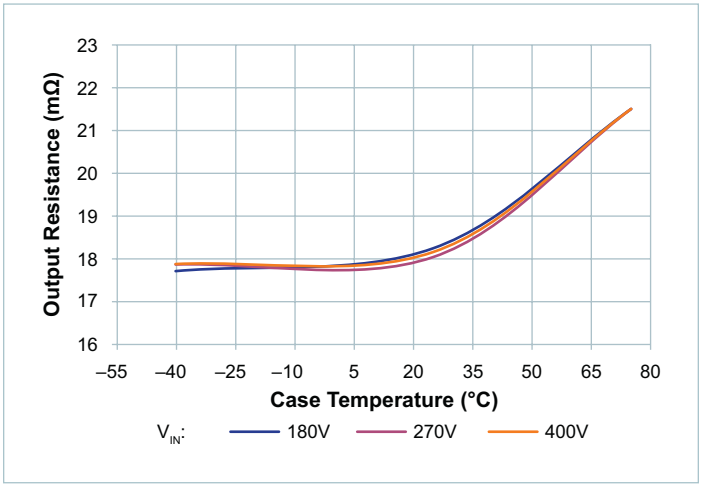


Figure 14 — *R_{OUT} vs. temperature at nominal trim*

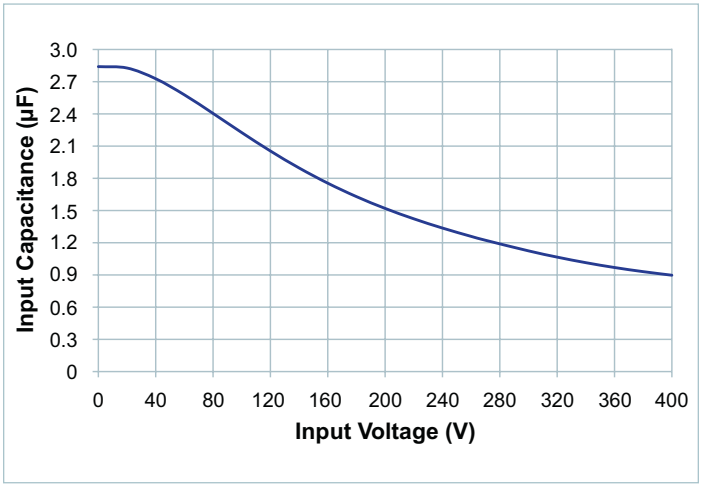


Figure 15 — *Effective internal input capacitance vs. V_{IN}*

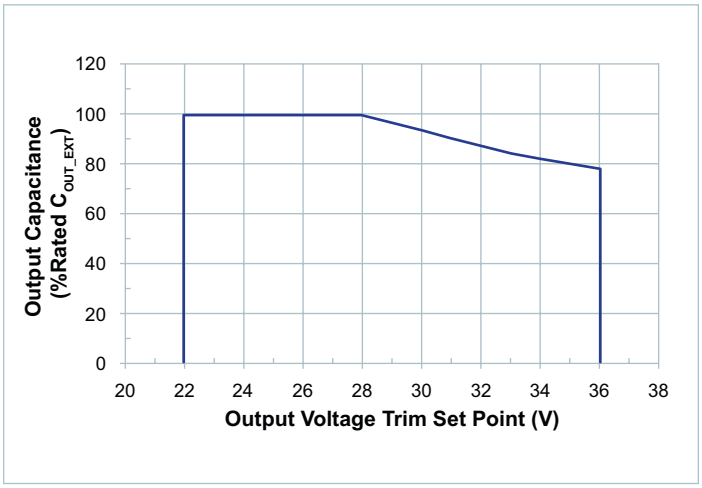


Figure 16 — *Maximum rated output capacitance $C_{OUT-EXT}$ at start up, over all line, no load*

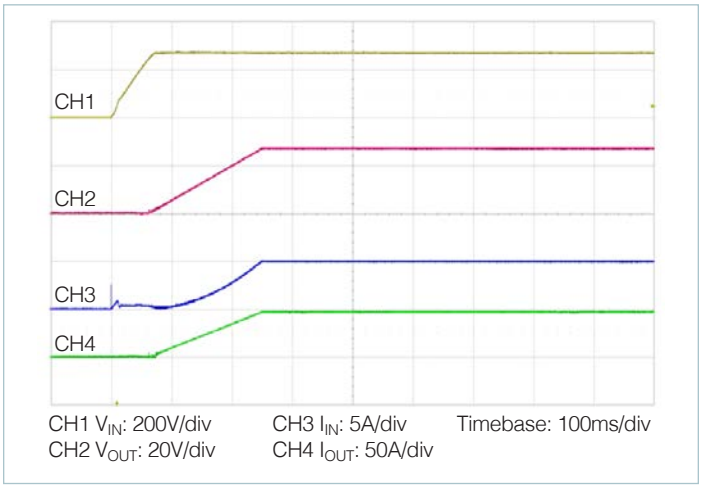


Figure 17 — *Input voltage start up, V_{IN} = 270V, V_{OUT} = 28V, C_{OUT_EXT} = 0F, R_{LOAD} = 0.6Ω*

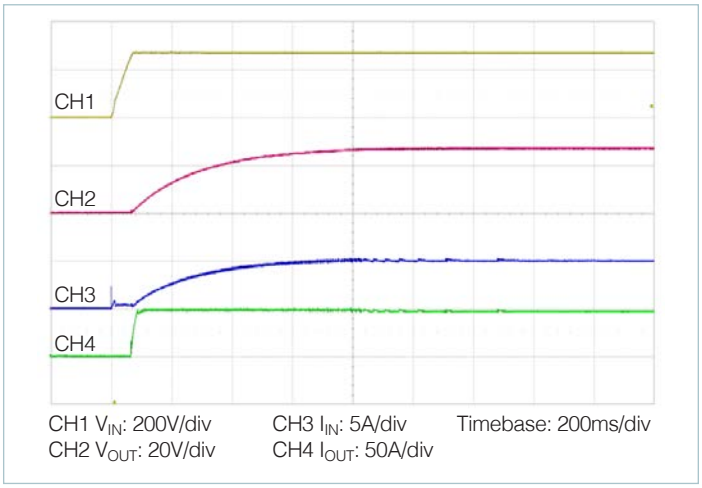


Figure 18 — *Input voltage start up, V_{IN} = 270V, V_{OUT} = 28V, C_{OUT_EXT} = 0.5F, R_{LOAD} = 0.6Ω*

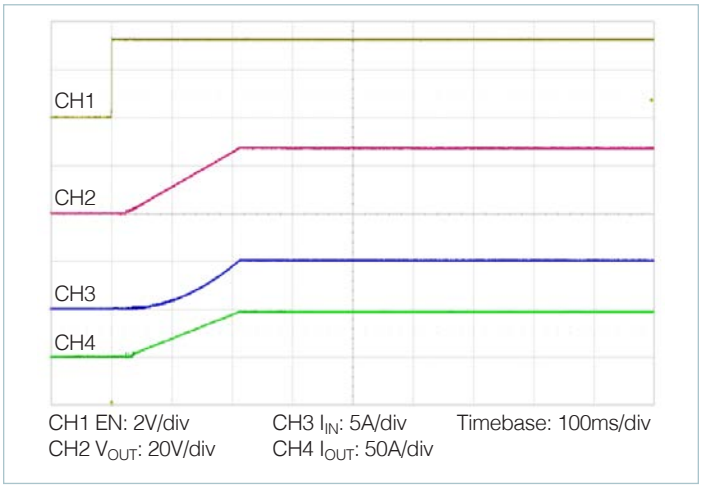


Figure 19 — *Start up from EN, V_{IN} = 270V, V_{OUT} = 28V, C_{OUT_EXT} = 0F, R_{LOAD} = 0.6Ω; analog-interface models only*

Application Characteristics (Cont.)

Temperature controlled via non-pin-side cold plate, unless otherwise noted. See associated figures for general trend data.

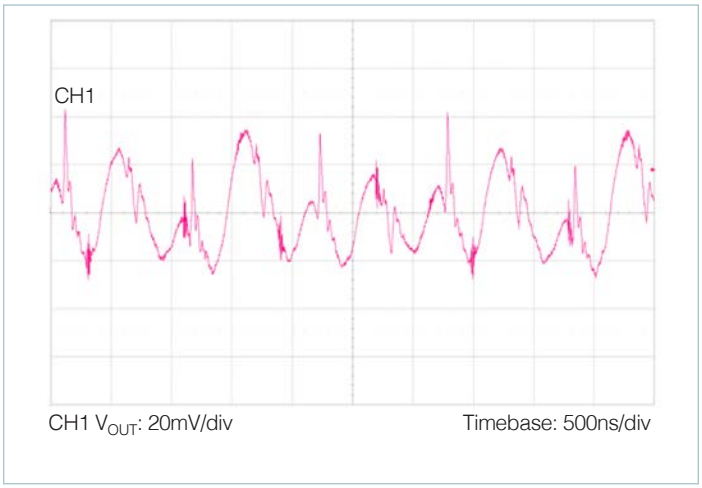


Figure 20 — *Output voltage ripple, V_{IN} = 270V, V_{OUT} = 28V, C_{OUT_EXT} = 0F, R_{LOAD} = 0.6Ω*

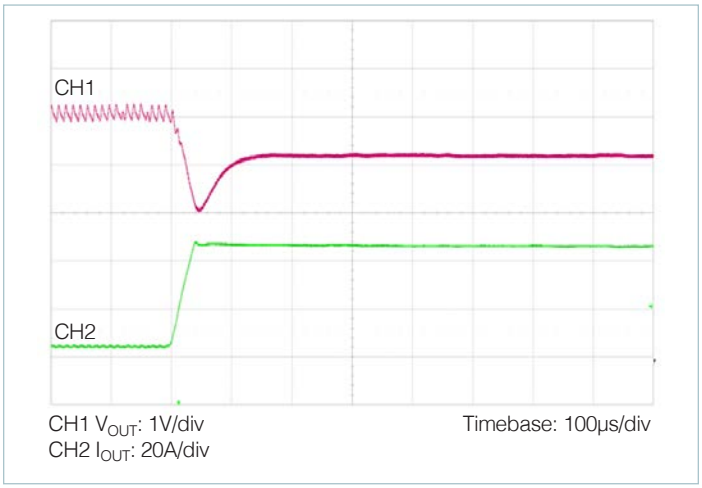


Figure 21 — *10 – 100% load transient response, V_{IN} = 270V, nominal trim, C_{OUT_EXT} = 0µF*

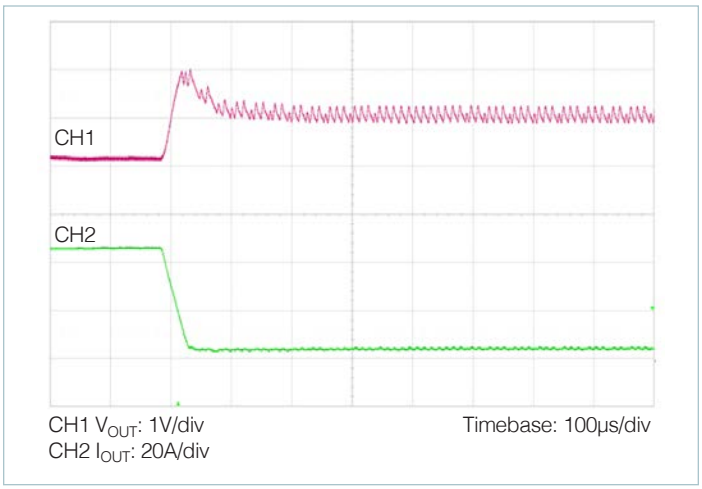


Figure 22 — *100 – 10% load transient response, V_{IN} = 270V, nominal trim, C_{OUT_EXT} = 0µF*

General Characteristics

Specifications apply over all line and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical [d]						
Length	L		141.18 [5.56]	141.43 [5.57]	141.68 [5.58]	mm [in]
Width	W		35.29 [1.39]	35.54 [1.40]	35.79 [1.41]	mm [in]
Height	H		9.02 [0.355]	9.40 [0.37]	9.78 [0.385]	mm [in]
Volume	Vol	Without heat sink		47.33 [2.89]		cm^3 [in^3]
Weight	W			215 [7.58]		g [oz]
Pin Material		C145 Copper				
Underplate		Low-stress ductile Nickel	50		100	µin
Pin Finish (Gold)		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Pin Finish (Tin)		Whisker-resistant-matte Tin	200		400	µin
Thermal						
Operating Internal Temperature [e]	T_{INT}	T-Grade	–40		125	°C
Thermal Resistance Pin Side	$\theta_{INT\_PIN\_SIDE}$	Estimated thermal resistance to maximum temperature internal component from isothermal pin/ terminal-side housing		0.97		°C/W
Thermal Resistance Housing	θ_{HOU}	Estimated thermal resistance of thermal coupling between the pin-side and non-pin-side case surfaces		0.42		°C/W
Thermal Resistance Non-Pin Side	$\theta_{INT\_NON\_PIN\_SIDE}$	Estimated thermal resistance to maximum temperature internal component from isothermal non-pin/ non-terminal housing		0.62		°C/W
Assembly						
Storage Temperature	T_{ST}	T-Grade	–40		125	°C
ESD Rating	HBM	Method per Human Body Model Test ESDA/JEDEC JDS-001-2012	CLASS 2			
	CDM	Charged Device Model JESD22-C101E	CLASS 2			
Soldering [f]						
Peak Temperature Top Case		For further information, please contact factory applications			130	°C

[d] Product appearance may change over time depending upon environmental exposure. This change has no impact on product performance.
[e] Temperature refers to the internal operation of the DCM. For maximum case temperature, please refer to Figure 1.
[f] Product is not intended for reflow solder attach.

General Characteristics (Cont.)

Specifications apply over all line and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range specified by the product grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Dielectric Withstand Test	V_{HIPOT}	IN to OUT	**2121**			V_{DC}
		IN to CASE	**2121**			
		OUT to CASE	**707**			
Reliability						
MTBF		MIL-HDBK-217Plus Parts Count 25°C Ground Benign, Stationary, Indoors / Computer		0.88		MHrs
		Telcordia Issue 2, Method I Case III, 25°C, Ground Benign, Controlled		1.85		MHrs
Agency Approvals						
Agency Approvals / Standards						
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Pin Functions – Standard Trim Options

Applies to all part numbers ***except*** DCM5614BD0H36K3TA9.

Power Terminals

+IN, –IN
Input power pins.

+OUT, –OUT
Output power pins. –OUT also serves as the reference for the secondary-referenced control pins on analog interface models.

Analog Signal Control Pins

EN (Enable)
This pin enables and disables the DCM converter; when held low the unit will be disabled. It is referenced to the –OUT pin of the converter. EN is active only if VDDE is pre-applied before V_{IN} is applied. Otherwise, EN is inactive and will be ignored until V_{IN} is removed and reapplied.

- Output enable: When EN is allowed to pull up above the enable threshold, the module will be enabled. If leaving EN floating, it is pulled up to V_{CC} and the module will be enabled.
- Output disable: EN may be pulled down externally in order to disable the module.
- EN is an input only, it does not pull low in the event of a fault.

TR (TRIM)
The TR pin is used to select the trim mode and to trim the output voltage when VDDE or V_{IN} is initially applied to the DCM converter.

The TR pin has an internal pull-up, R_{TRIM_INT}, to VCC. The DCM converter in TRIM active mode will not allow real time trimming of the output voltage.

- *Without VDDE pre-applied*
  The DCM will latch trim behavior at application of V_{IN} (once V_{IN} exceeds $V_{IN\text{-}UVLO+}$), and persist in that same behavior until loss of input voltage.
  - **TRIM inactive:** at application of V_{IN}, if TR is sampled at a value above $V_{TRIM\text{-}DIS}$, the module will latch in a non-trim mode, and will ignore the TR input for as long as V_{IN} is present.
  - **TRIM active:** at application of V_{IN}, if TR is sampled at a value below $V_{TRIM\text{-}EN}$, the TR will serve as an input to set the output voltage permanently to a sampled trim level. It will persist in this behavior until V_{IN} is no longer present and V_{OUT} falls below the internal controller reset voltage, $V_{OUT\text{-}MICRO\text{-}RESET}$. The DCM converter in this mode will ignore the TR input for as long as V_{IN} is present.

TR also decreases the current limit threshold when the trim set point is above $V_{OUT\text{-}NOM}$.

- *With VDDE pre-applied:*
  When the VDDE is first applied before the application of V_{IN}, the DCM will latch trim behavior and persist in that same behavior until loss of V_{IN}, and both VDDE, V_{OUT} falls below the respective internal controller reset voltages, $V_{VDDE\text{-}MICRO\text{-}RESET}$ and $V_{OUT\text{-}MICRO\text{-}RESET}$.
  - **TRIM inactive:** Before the application of V_{IN} and at initial application of VDDE, if TR is sampled at a value above $V_{TRIM\text{-}DIS}$, the module will latch in a non-trim mode and will ignore the TR input for as long as VDDE and V_{IN} are present.
  - **TRIM active:** Before the application of VIN and at initial application of VDDE, if TR is sampled at a value below $V_{TRIM\text{-}EN}$, the TR will serve as an input to set the output voltage permanently to a sampled trim level. It will persist in this behavior until loss of VIN, and both VDDE, V_{OUT} falls below the respective internal controller reset voltages, $V_{VDDE\text{-}MICRO\text{-}RESET}$ and $V_{OUT\text{-}MICRO\text{-}RESET}$. The DCM converter in this mode will not allow real time trimming of the output voltage. TR also decreases the current limit threshold when the trim set point is above $V_{OUT\text{-}NOM}$.

PMBus® Signal Control Pins

SCL and SDA (Serial Clock and Serial Data)
I^2C communication signal pin interface for PMBus Host clock and data connection. SCL and SDA are not internally pulled up to any voltage, permitting flexibility for the user in defining the communication bus voltage. External pull-up resistors are required, the value of which should be considered dependent on the SCL and SDA signal routing impedance characteristics.

ADDR (Address)
This pin programs the module with a fixed and persistent PMBus address using a resistor between the ADDR pin and SGND. The address pin has an internal 10kΩ pull-up resistor to V_{CC}. The address is sampled by the DCM's internal microcontroller at initial turn on and held until power is removed. See the Device Address table in the PMBus Interface section for recommended values of R_{ADDR}.

Please note: For chassis mount models, Vicor part number 42550 will be needed for applications requiring the use of signal pins.

Pin Functions – Dynamic Trim Option

Applies to part number DCM5614BD0H36K3TA9 only.

Power Terminals

+IN, –IN
Input power pins.

+OUT, –OUT
Output power pins. –OUT also serves as the reference for the secondary-referenced control pins on analog interface models.

Analog Signal Control Pins

EN (Enable)
This pin enables and disables the DCM converter; when held low the unit will be disabled. It is referenced to the –OUT pin of the converter. EN is active only if VDDE is pre-applied before V_{IN} is applied. Otherwise, EN is inactive and will be ignored until V_{IN} is removed and reapplied.

- Output enable: When EN is allowed to pull up above the enable threshold, the module will be enabled. If leaving EN floating, it is pulled up to V_{CC} and the module will be enabled.
- Output disable: EN may be pulled down externally in order to disable the module.
- EN is an input only, it does not pull low in the event of a fault.

TR (TRIM)
The TR pin is used to select the trim mode and to trim the output voltage of the DCM converter. The TR pin has an internal pull-up to V_{CC}.

The DCM will latch trim behavior at application of V_{IN} (once V_{IN} exceeds $V_{IN\text{-}UVLO+}$), and persist in that same behavior until loss of input voltage.

- At application of V_{IN}, if TR is sampled at a value above $V_{TRIM\text{-}DIS}$, the module will latch in a non-trim mode, and will ignore the TR input for as long as V_{IN} is present.
- At application of V_{IN}, if TR is sampled at a value below $V_{TRIM\text{-}EN}$, the TR will serve as an input to control the real time output voltage. It will persist in this behavior until V_{IN} is no longer present.

If trim is active when the DCM is operating, the TR pin provides dynamic trim control at a typical 0.4Hz of –3dB bandwidth over the output voltage. TR also decreases

PMBus® Signal Control Pins

SCL and SDA (Serial Clock and Serial Data)
I^2C™ communication signal pin interface for PMBus Host clock and data connection. SCL and SDA are not internally pulled up to any voltage, permitting flexibility for the user in defining the communication bus voltage. External pull-up resistors are required, the value of which should be considered dependent on the SCL and SDA signal routing impedance characteristics.

ADDR (Address)
This pin programs the module with a fixed and persistent PMBus address using a resistor between the ADDR pin and SGND. The address pin has an internal 10kΩ pull-up resistor to V_{CC}. The address is sampled by the DCM's internal microcontroller at initial turn on and held until power is removed. See the Device Address table in the PMBus Interface section for recommended values of R_{ADDR}.

Please note: For chassis mount models, Vicor part number 42550 will be needed for applications requiring the use of signal pins.

Design Guidelines – Standard Trim Options

Applies to all part numbers ***except*** DCM5614BD0H36K3TA9.

Building Blocks and System Design

The DCM converter input accepts the full 180 – 400V range, and it generates an isolated trimmable 28.0V_{DC} output. Multiple DCMs may be paralleled for higher power capacity via wireless load sharing, even when they are operating off of different input voltage supplies.

The DCM converter provides a regulated output voltage with a load dependent, resistive droop characteristic (R_{OUT}). The load line enables configuration of an array of DCM converters that manage the output load with no share signal bus among modules. When multiple DCM5614 modules are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point-of-load. Ensuring equal current sharing among modules requires that DCM array impedances be matched. Downstream regulators may be used to provide tighter voltage regulation if required.

The DCM5614xD0H36K3yzz may be used in standalone applications where the output power requirements are up to 1300W. However, it is easily deployed as arrays of modules to increase power handling capacity. Arrays of up to four units have been qualified for 5.2kW capacity. Application of DCM converters in an array requires no de-rating of the maximum available power versus what is specified for a single module. To ensure reliable system recovery in the event of a fault of one or more units in an array, ORing of the DCM outputs is needed. Note that the addition of ORing circuitry can influence current sharing among modules.

Soft Start

When the DCM starts, it will go through a soft start. The soft-start routine ramps the output voltage by modulating the internal error amplifier reference. This causes the output voltage to approximate a piecewise linear ramp. The output ramp finishes when the voltage reaches either the nominal output voltage or the trimmed output voltage as set by either the TR pin (analog interface modules) or the VOUT_COMMAND (21h – PMBus interface modules). The DCM is capable of supporting full rated output current during start up and will enter constant-current operation to support charging highly capacitive loads (see Figure 16).

Trim Mode and Output Trim Control (Analog Interface Modules)

The TR pin has an internal pull-up resistor, R_{TRIM_INT}, to VCC, so unless external circuitry pulls the pin voltage lower, it will pull up to VCC.

Without VDDE pre-applied:
When the input voltage is initially applied to a DCM, and after t_{INIT} elapses, the trim pin voltage V_{TR} is sampled.

With VDDE pre-applied:
When the VDDE is initially applied before the application of VIN to a DCM, the trim pin voltage V_{TR} is sampled.

If the initially sampled trim pin voltage is higher than $V_{TRIM-DIS}$ with either VDDE or V_{IN} first applied, the DCM will disable trimming of the output voltage.

In this case, for all subsequent operation, the output voltage will be set to the nominal set point, $V_{OUT-NOM}$. This minimizes the support components required for applications that only require the nominal rated V_{OUT} and also provides the best output set-point accuracy as there are no additional errors introduced from external trim components.

If, at initial application of VDDE or V_{IN}, the TR pin voltage is prevented from exceeding $V_{TRIM-EN}$, then the DCM will sample the trim pin voltage and sets the output voltage permanently to the sampled trim value and will remain in this mode for as long as VDDE and V_{IN} is applied. In this mode, the DCM converter will not allow real-time trimming of the output voltage.

V_{OUT} set point at no load can be calculated using the equation below:

$$V_{OUT\text{-}TRIMMING} = 20.00 + \left(20.625 \bullet \frac{V_{TR}}{V_{CC}}\right) \qquad (1)$$

Note: the trim mode is not changed when a DCM recovers from any fault condition or being disabled.

Module performance is guaranteed through output voltage trim range $V_{OUT-TRIMMING}$. If V_{OUT} is trimmed above this range, then certain combinations of line and load transient conditions may trigger the output OVP.

Output Current Limit

The DCM features a fully operational firmware-controlled current limit that effectively keeps the module operating inside the Safe Operating Area (SOA) for all valid trim and load profiles. The current limit approximates a "brick wall" limit, where the output current is prevented from exceeding the current limit threshold by reducing the output voltage via the internal error amplifier reference.

Sustained operation in current limit is permitted and no de-rating of output power is required. In order to preserve the SOA, when the converter is trimmed above the nominal output voltage, the current limit threshold is automatically reduced to limit the available output power.

Current limit can reduce the output voltage to as little as the UVP threshold ($V_{OUT-UVP}$). Below this minimum output voltage compliance level, further loading will cause the module to shut down due to the output undervoltage fault protection.

Analog Interface Modules

The current limit threshold at all trim conditions is 105% of rated output current. Note that at output voltage trim conditions higher than 28V, the rated output current is automatically reduced to prevent exceeding the 1300W rated output power capability of the module. The module may enter current-limited operation during soft start when charging large capacitive loads (see Figure 16).

PMBus® Interface Modules

The default current limit threshold at all trim conditions is 105% of rated output current. Note that at output voltage trim conditions higher than 28V, the rated output current is automatically reduced to prevent exceeding the 1300W rated output power capability of the module. The current limit threshold may be adjusted from 0 to 105% of rated current via the MFR_CONSTANT_CURRENT (E8h) command, see PMBus Interface section beginning on page 25. This command also permits disabling the firmware-controlled constant-current behavior such that an output overcurrent event exceeding I_{OUT_CL} triggers the hardware overcurrent protection and disables the powertrain for a minimum time t_{CL_FAULT}. The module will periodically attempt to restart until the overcurrent condition is removed and normal operation resumes.

The module may enter current-limited operation during soft start when charging large capacitive loads (see Figure 16). The current limit threshold during soft start is set according to the MFR_CONSTANT_CURRENT (E8h). Current-limited operation during soft start is retained (105% threshold) even if the firmware-controlled constant-current behavior is disabled.

Line Impedance, Input Slew rate and Input Stability Requirements

Connect a high-quality, low-noise power supply to the +IN and –IN terminals. Additional capacitance may have to be added between +IN and –IN to make up for impedances in the interconnect cables as well as deficiencies in the source.

Excessive source impedance can bring about system stability issues for a regulated DC-DC converter, and must either be avoided or compensated. A 100µF input capacitor is the minimum recommended in case the source impedance is insufficient to satisfy stability requirements.

Additional information can be found in the filter design application note.

Please refer to this input filter design tool to ensure input stability.

Ensure that the input voltage slew rate is less than 1V/µs, otherwise a pre-charge circuit is required for the DCM input to control the input voltage slew rate and prevent overstress to input stage components.

Input Fuse Selection

The DCM is not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at the system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than the DCM converter's maximum current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting I^2t
- Recommended fuse: Littelfuse® 487 series rated 10A.

Fault Handling

The following section describes fault conditions in which the DCM will automatically shut down to protect the powertrain from operation outside the prescribed safe operating area. All faults are non-latching; the powertrain will automatically attempt to restart once the fault condition subsides.

Input Undervoltage Fault Protection (UVLO)
The converter's input voltage is monitored to detect an input undervoltage condition. If the converter is not already running, then it will ignore enable commands until the input voltage is greater than $V_{IN-UVLO+}$. If the converter is running and the input voltage falls below $V_{IN-UVLO-}$, the converter recognizes a fault condition, the powertrain stops switching, and the output voltage of the unit falls.

Input voltage transients which fall below UVLO for less than t_{UVLO} may not be detected by the fault protection logic, in which case the converter will continue regular operation. No protection is required in this case.

Once the UVLO fault is detected by the fault protection logic, the converter shuts down and waits for the input voltage to rise above $V_{IN-UVLO+}$. Provided the converter is still enabled, it will then restart.

Input Overvoltage Fault Protection (OVLO)
The converter's input voltage is monitored to detect an input overvoltage condition. When the input voltage is higher than $V_{IN-OVLO+}$, a fault is detected, the powertrain stops switching, and the output voltage of the converter falls.

After an OVLO fault occurs, the converter will wait for the input voltage to fall below $V_{IN-OVLO-}$. Provided the converter is still enabled, the powertrain will restart.

A time dependent overvoltage protection permits the module to ride through short duration voltage surge transients. The converter will continue to process power so long as the input voltage returns to a level below $V_{IN-OVLO-}$ within t_{OVLO}.

Output Undervoltage Fault Protection (UVP)
The converter determines that an output overload or short circuit condition exists by measuring its output voltage and the output of the internal error amplifier. In general, whenever the powertrain is switching and the output voltage falls below $V_{OUT-UVP}$ threshold, a undervoltage fault will be registered. Once an output undervoltage condition is detected, the powertrain immediately stops switching, and the output voltage of the converter falls. The converter remains disabled for a time t_{FAULT}. Once recovered and provided the converter is still enabled, the powertrain will restart.

Temperature Fault Protections (OTP)

The fault logic monitors the internal temperature of the converter. If the measured temperature exceeds $T_{INT-OTP}$, a temperature fault is registered. As with the undervoltage fault protection, once a temperature fault is registered, the powertrain immediately stops switching, the output voltage of the converter falls, and the converter remains disabled for at least time $t_{OTP-FAULT}$. Then, the converter waits for the internal temperature to return to below $T_{INT-OTP}$ before recovering. Provided the converter is still enabled, the DCM will restart.

Output Overvoltage Fault Protection (OVP)

The converter monitors the output voltage during each switching cycle. If the output voltage exceeds $V_{OUT-OVP+}$, the OVP fault protection is triggered. The control logic disables the powertrain, and the output voltage of the converter falls.

The DCM will remain disabled for at least time t_{FAULT}. Provided the converter is still enabled and the output voltage has fallen below $V_{OUT-OVP-}$, the powertrain will restart.

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the pin-side surface, the non-pin-side surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a DCM in a VIA package, as can be seen from specified thermal operating area on Page 4. Since the VIA package has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. To this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 23 shows the "thermal circuit" for the VIA package.

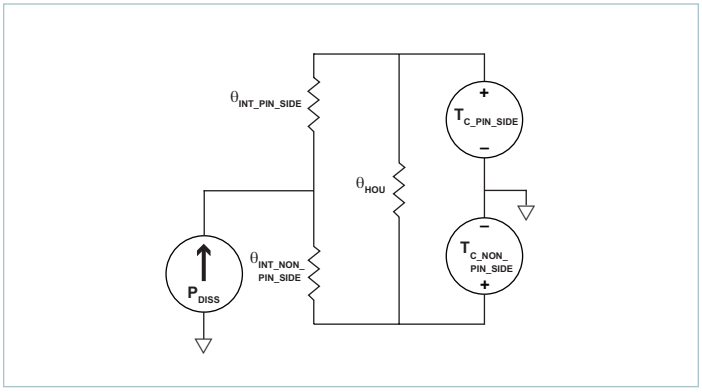


Figure 23 — *Double-sided cooling thermal model*

In this case, the internal power dissipation is P_{DISS}, $\theta_{INT\_PIN\_SIDE}$ and $\theta_{INT\_NON\_PIN\_SIDE}$ are thermal resistance characteristics of the VIA package and the pin-side and non-pin-side surface temperatures are represented as $T_{C\_PIN\_SIDE}$, and $T_{C\_NON\_PIN\_SIDE}$. It is interesting to notice that the package itself provides a high degree of thermal coupling between the pin-side and non-pin-side case surfaces (represented in the model by the resistor θ_{HOU}). This feature enables two main options regarding thermal designs:

Single-side cooling: the model of Figure 23 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for non-pin-side cooling only is shown in Figure 24.

In this case, θ_{INT} can be derived as following:

$$\theta_{INT} = \frac{\left(\theta_{INT\_PIN\_SIDE} + \theta_{HOU}\right) \bullet \theta_{INT\_NON\_PIN\_SIDE}}{\theta_{INT\_PIN\_SIDE} + \theta_{HOU} + \theta_{INT\_NON\_PIN\_SIDE}} \qquad (2)$$

Double-side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, like for example heatsinks with independent airflows or a combination of chassis/air cooling.

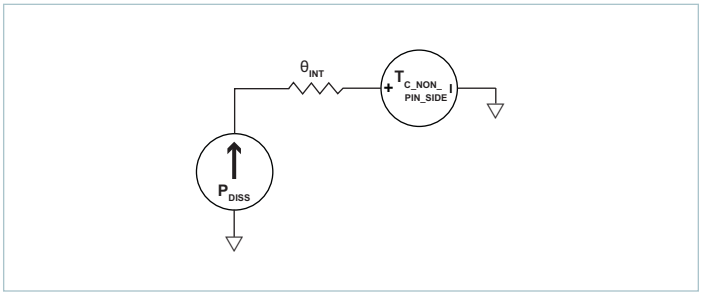


Figure 24 — *Single-sided cooling thermal model*

Grounding Considerations

The chassis of the DCM is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products.

Dielectric Withstand

The DCM contains an internal safety approved isolating component (ChiP™) that provides the Reinforced Insulation from Input to Output. The isolating component is individually tested for Reinforced Insulation from Input to Output at $4242V_{DC}$ prior to the final assembly of the DCM in a VIA package.

When the VIA package assembly is complete the Reinforced Insulation can only be tested at Basic Insulation values as specified in the electric strength Test Procedure noted in clause 5.2.2 of IEC 60950-1.

Test Procedure Note from IEC 60950-1

"For equipment incorporating both REINFORCED INSULATION and lower grades of insulation, care is taken that the voltage applied to the REINFORCED INSULATION does not overstress BASIC INSULATION or SUPPLEMENTARY INSULATION."

Summary

The final package assembly contains basic insulation from input to case, reinforced insulation from input to output, and functional insulation from output to case.

The output of the DCM complies with the requirements of SELV circuits so only functional insulation is required from the output

(SELV) to case (PE) because the case is required to be connected to protective earth in the final installation. The construction of the DCM in a VIA package can be summarized by describing it as a "Class II" component installed in a "Class I" subassembly. The reinforced insulation from input to output can only be tested at a basic insulation value of $2121V_{DC}$ on the completely assembled VIA package.

Design Guidelines – Dynamic Trim Option

Applies to part number DCM5614BD0H36K3TA9 only.

Building Blocks and System Design

The DCM converter input accepts the full 180 – 400V range, and it generates an isolated trimmable 28.0V_{DC} output. Multiple DCMs may be paralleled for higher power capacity via wireless load sharing, even when they are operating off of different input voltage supplies.

The DCM converter provides a regulated output voltage with a load dependent, resistive droop characteristic (R_{OUT}). The load line enables configuration of an array of DCM converters that manage the output load with no share signal bus among modules. When multiple DCM5614 modules are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point-of-load. Ensuring equal current sharing among modules requires that DCM array impedances be matched. Downstream regulators may be used to provide tighter voltage regulation if required.

The VIZ2022 may be used in standalone applications where the output power requirements are up to 1300W. However, it is easily deployed as arrays of modules to increase power handling capacity. Arrays of up to four units have been qualified for 5.2kW capacity. Application of DCM converters in an array requires no de-rating of the maximum available power versus what is specified for a single module. To ensure reliable system recovery in the event of a fault of one or more units in an array, ORing of the DCM outputs is needed. Note that the addition of ORing circuitry can influence current sharing among modules.

Soft Start

When the DCM starts, it will go through a soft start. The soft-start routine ramps the output voltage by modulating the internal error amplifier reference. This causes the output voltage to approximate a piecewise linear ramp. The output ramp finishes when the voltage reaches either the nominal output voltage or the trimmed output voltage as set by either the TR pin (analog interface modules) or the VOUT_COMMAND (21h – PMBus interface modules). The DCM is capable of supporting full rated output current during start up and will enter constant-current operation to support charging highly capacitive loads (see Figure 16).

Trim Mode and Output Trim Control (Analog Interface Modules)

When the input voltage is initially applied to a DCM, and after t_{INIT} elapses, the trim pin voltage V_{TR} is sampled. The TR pin has an internal pull-up resistor to V_{CC}, so unless external circuitry

pulls the pin voltage lower, it will pull up to V_{CC}. If the initially sampled trim pin voltage is higher than $V_{TRIM-DIS}$, then the DCM will disable trimming as long as V_{IN} remains applied. In this case, for all subsequent operation, the output voltage will be programmed to the nominal set point. This minimizes the support components

required for applications that only require the nominal rated V_{OUT} and also provides the best output set-point accuracy as there are no additional errors introduced from external trim components.

If, at initial application of V_{IN}, the TR pin voltage is prevented from exceeding $V_{TRIM-EN}$, then the DCM will activate trim mode. The trim mode will remain active for as long as V_{IN} is applied.

V_{OUT} set point at no load can be calculated using the equation below:

$$V_{OUT\text{-}TRIMMING} = 20.00 + \left(20.625 \bullet \frac{V_{TR}}{V_{CC}}\right) \quad (1)$$

Note: the trim mode is not changed when a DCM recovers from any fault condition or being disabled.

Module performance is guaranteed through output voltage trim range $V_{OUT\text{-}TRIMMING}$. If V_{OUT} is trimmed above this range, then certain combinations of line and load transient conditions may trigger the output OVP.

Output Current Limit

The DCM features a fully operational firmware-controlled current limit that effectively keeps the module operating inside the Safe Operating Area (SOA) for all valid trim and load profiles. The current limit approximates a "brick wall" limit, where the output current is prevented from exceeding the current limit threshold by reducing the output voltage via the internal error amplifier reference.

Sustained operation in current limit is permitted and no de-rating of output power is required. In order to preserve the SOA, when the converter is trimmed above the nominal output voltage, the current limit threshold is automatically reduced to limit the available output power.

Current limit can reduce the output voltage to as little as the UVP threshold ($V_{OUT\text{-}UVP}$). Below this minimum output voltage compliance level, further loading will cause the module to shut down due to the output undervoltage fault protection.

Analog Interface Modules

The current limit threshold at all trim conditions is 105% of rated output current. Note that at output voltage trim conditions higher than 28V, the rated output current is automatically reduced to prevent exceeding the 1300W rated output power capability of the module. The module may enter current-limited operation during soft start when charging large capacitive loads (see Figure 16).

PMBus® Interface Modules

The default current limit threshold at all trim conditions is 105% of rated output current. Note that at output voltage trim conditions higher than 28V, the rated output current is automatically reduced to prevent exceeding the 1300W rated output power capability of the module. The current limit threshold may be adjusted from 0 to 105% of rated current via the MFR_CONSTANT_CURRENT (E8h) command, see PMBus Interface section beginning on page 25. This command also permits disabling the firmware-controlled constant-current behavior such that an output overcurrent event exceeding I_{OUT_CL} triggers the hardware overcurrent protection and disables the powertrain for a minimum time t_{CL_FAULT}. The module will periodically attempt to restart until the overcurrent condition is removed and normal operation resumes.

The module may enter current-limited operation during soft start when charging large capacitive loads (see Figure 16). The current limit threshold during soft start is set according to the MFR_CONSTANT_CURRENT (E8h). Current-limited operation during soft start is retained (105% threshold) even if the firmware-controlled constant-current behavior is disabled.

Line Impedance, Input Slew rate and Input Stability Requirements

Connect a high-quality, low-noise power supply to the +IN and –IN terminals. Additional capacitance may have to be added between +IN and –IN to make up for impedances in the interconnect cables as well as deficiencies in the source.

Excessive source impedance can bring about system stability issues for a regulated DC-DC converter, and must either be avoided or compensated. A 100µF input capacitor is the minimum recommended in case the source impedance is insufficient to satisfy stability requirements.

Additional information can be found in the filter design application note.

Please refer to this input filter design tool to ensure input stability.

Ensure that the input voltage slew rate is less than 1V/µs, otherwise a pre-charge circuit is required for the DCM input to control the input voltage slew rate and prevent overstress to input stage components.

Input Fuse Selection

The DCM is not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at the system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than the DCM converter's maximum current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting I^2t
- Recommended fuse: Littelfuse® 487 series rated 10A.

Fault Handling

The following section describes fault conditions in which the DCM will automatically shut down to protect the powertrain from operation outside the prescribed safe operating area. All faults are non-latching; the powertrain will automatically attempt to restart once the fault condition subsides.

Input Undervoltage Fault Protection (UVLO)
The converter's input voltage is monitored to detect an input undervoltage condition. If the converter is not already running, then it will ignore enable commands until the input voltage is greater than $V_{IN\text{-}UVLO+}$. If the converter is running and the input voltage falls below $V_{IN\text{-}UVLO–}$, the converter recognizes a fault condition, the powertrain stops switching, and the output voltage of the unit falls.

Input voltage transients which fall below UVLO for less than t_{UVLO} may not be detected by the fault protection logic, in which case the converter will continue regular operation. No protection is required in this case.

Once the UVLO fault is detected by the fault protection logic, the converter shuts down and waits for the input voltage to rise above $V_{IN\text{-}UVLO+}$. Provided the converter is still enabled, it will then restart.

Input Overvoltage Fault Protection (OVLO)
The converter's input voltage is monitored to detect an input overvoltage condition. When the input voltage is higher than $V_{IN\text{-}OVLO+}$, a fault is detected, the powertrain stops switching, and the output voltage of the converter falls.

After an OVLO fault occurs, the converter will wait for the input voltage to fall below $V_{IN\text{-}OVLO–}$. Provided the converter is still enabled, the powertrain will restart.

A time dependent overvoltage protection permits the module to ride through short duration voltage surge transients. The converter will continue to process power so long as the input voltage returns to a level below $V_{IN\text{-}OVLO–}$ within t_{OVLO}.

Output Undervoltage Fault Protection (UVP)
The converter determines that an output overload or short circuit condition exists by measuring its output voltage and the output of the internal error amplifier. In general, whenever the powertrain is switching and the output voltage falls below $V_{OUT\text{-}UVP}$ threshold, a undervoltage fault will be registered. Once an output undervoltage condition is detected, the powertrain immediately stops switching, and the output voltage of the converter falls. The converter remains disabled for a time t_{FAULT}. Once recovered and provided the converter is still enabled, the powertrain will restart.

Temperature Fault Protections (OTP)

The fault logic monitors the internal temperature of the converter. If the measured temperature exceeds $T_{INT\text{-}OTP}$, a temperature fault is registered. As with the undervoltage fault protection, once a temperature fault is registered, the powertrain immediately stops switching, the output voltage of the converter falls, and the converter remains disabled for at least time $t_{OTP\text{-}FAULT}$. Then, the converter waits for the internal temperature to return to below $T_{INT\text{-}OTP}$ before recovering. Provided the converter is still enabled, the DCM will restart.

Output Overvoltage Fault Protection (OVP)

The converter monitors the output voltage during each switching cycle. If the output voltage exceeds $V_{OUT\text{-}OVP+}$, the OVP fault protection is triggered. The control logic disables the powertrain, and the output voltage of the converter falls.

The DCM will remain disabled for at least time t_{FAULT}. Provided the converter is still enabled and the output voltage has fallen below $V_{OUT\text{-}OVP–}$, the powertrain will restart.

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the pin-side surface, the non-pin-side surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a DCM in a VIA package, as can be seen from specified thermal operating area on Page 4. Since the VIA package has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. To this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 23 shows the "thermal circuit" for the VIA package.

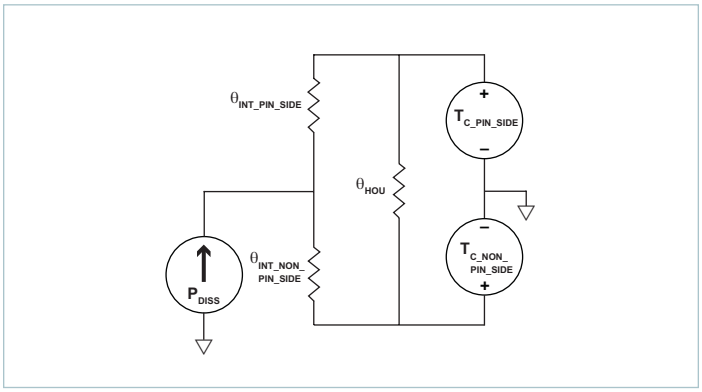


Figure 25 — *Double-sided cooling thermal model*

In this case, the internal power dissipation is P_{DISS}, $\theta_{INT\_PIN\_SIDE}$ and $\theta_{INT\_NON\_PIN\_SIDE}$ are thermal resistance characteristics of the VIA package and the pin-side and non-pin-side surface temperatures are represented as $T_{C\_PIN\_SIDE}$, and $T_{C\_NON\_PIN\_SIDE}$. It is interesting to notice that the package itself provides a high degree of thermal coupling between the pin-side and non-pin-side case surfaces (represented in the model by the resistor θ_{HOU}). This feature enables two main options regarding thermal designs:

Single-side cooling: the model of Figure 25 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for non-pin-side cooling only is shown in Figure 26.

In this case, θ_{INT} can be derived as following:

$$\theta_{INT} = \frac{\left(\theta_{INT\_PIN\_SIDE} + \theta_{HOU}\right) \bullet \theta_{INT\_NON\_PIN\_SIDE}}{\theta_{INT\_PIN\_SIDE} + \theta_{HOU} + \theta_{INT\_NON\_PIN\_SIDE}} \qquad (2)$$

Double-side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, like for example heatsinks with independent airflows or a combination of chassis/air cooling.

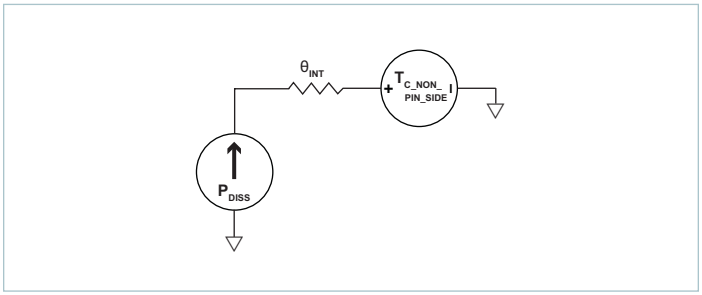


Figure 26 — *Single-sided cooling thermal model*

Grounding Considerations

The chassis of the DCM is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products.

Dielectric Withstand

The DCM contains an internal safety approved isolating component (ChiP™) that provides the Reinforced Insulation from Input to Output. The isolating component is individually tested for Reinforced Insulation from Input to Output at $4242V_{DC}$ prior to the final assembly of the DCM in a VIA package.

When the VIA package assembly is complete the Reinforced Insulation can only be tested at Basic Insulation values as specified in the electric strength Test Procedure noted in clause 5.2.2 of IEC 60950-1.

Test Procedure Note from IEC 60950-1

"For equipment incorporating both REINFORCED INSULATION and lower grades of insulation, care is taken that the voltage applied to the REINFORCED INSULATION does not overstress BASIC INSULATION or SUPPLEMENTARY INSULATION."

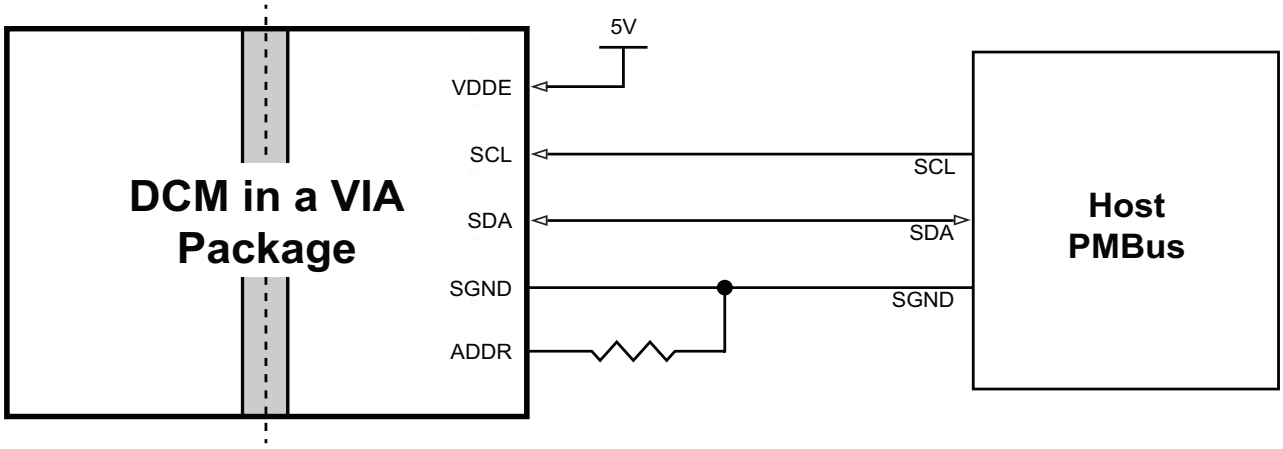
Summary

The final package assembly contains basic insulation from input to case, reinforced insulation from input to output, and functional insulation from output to case.

The output of the DCM complies with the requirements of SELV circuits so only functional insulation is required from the output

(SELV) to case (PE) because the case is required to be connected to protective earth in the final installation. The construction of the DCM in a VIA package can be summarized by describing it as a "Class II" component installed in a "Class I" subassembly. The reinforced insulation from input to output can only be tested at a basic insulation value of $2121V_{DC}$ on the completely assembled VIA package.

System Diagram for PMBus® Interface



The controller of the DCM in a VIA package is referenced to the low-voltage-side signal ground (SGND).

The DCM in a VIA package provides the Host PMBus system with accurate telemetry monitoring and reporting, voltage and current setpoint adjustment, in addition to corresponding status flags. The standalone DCM is periodically polled for status by the host PMBus. Direct communication to the DCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the DCM controller data and page (0x01) prior to a telemetry inquiry points to the DCM parameters.

The DCM enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The DCM follows the PMBus command structure and specification.

PMBus® Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.3, Part I and II" for complete PMBus specifications details at https://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of a predetermined sixteen possible addresses shown in the table below using a resistor between ADDR pin and SGND pin.

The DCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power-up, the DCM internal microcontroller will sample the address pin voltage, and will hold this address until device power is removed.

ID	Child Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The DCM controller employs a direct data format where all reported measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the COEFFICIENTS command is not supported:

Where:

X is a "real world" value in units (A, V, °C, s)

Y is a two's complement integer received from the internal microcontroller

m, b and R are two's complement integers defined as follows:

$$X = \left(\frac{1}{m}\right) \bullet \left(Y \bullet 10^{-R} - b\right) \qquad (3)$$

Command	Code	m	R	b
VOUT_COMMAND	21h	1	2	0
READ_VIN	88h	1	1	0
READ_VOUT	8Bh	1	2	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1	8Dh	1	0	0
READ_POUT	96h	1	1	0
MFR_VIN_MIN	A0h	1	1	0
MFR_VIN_MAX	A1h	1	1	0
MFR_VOUT_MIN	A4h	1	2	0
MFR_VOUT_MAX	A5h	1	2	0
MFR_IOUT_MAX	A6h	1	2	0
MFR_POUT_MAX	A7h	1	1	0
MFR_POUT_MAX	A7h	1	0	0
MFR_CONSTANT_CURRENT	E8h	1	2	0

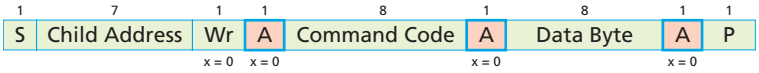
Supported Command List

Command	Code	Function	Default Data Content	Data Bytes
PAGE	00h	Access stored DCM information	00h	1
OPERATION	01h	Turn DCM on or off	80h	1
CLEAR_FAULTS	03h	Clear all faults	N/A	None
CAPABILITY	19h	PMBus® key capabilities set by factory	20h	1
VOUT_MODE	20h	Returns the format of the output voltage data	40h	1
VOUT_COMMAND	21h	Set DCM output voltage	V_{OUT} Nom	2
STATUS_BYTE	78h	Summary of faults	00h	1
STATUS_WORD	79h	Summary of fault conditions	00h	2
STATUS_VOUT	7Ah	Output overvoltage and undervoltage fault status	00h	1
STATUS_IOUT	7Bh	Overcurrent fault status	00h	1
STATUS_INPUT	7Ch	Input overvoltage and undervoltage fault status	00h	1
STATUS_TEMPERATURE	7Dh	Overtemperature and undertemperature fault status	00h	1
STATUS_CML	7Eh	PMBus communication fault	00h	1
STATUS_MFR_SPECIFIC	80h	Other DCM status indicator	00h	1
READ_VIN	88h	Read input voltage	FFFFh	2
READ_VOUT	8Bh	Read output voltage	FFFFh	2
READ_IOUT	8Ch	Read output current	FFFFh	2
READ_TEMPERATURE_1	8Dh	Read internal controller temperature	FFFFh	2
READ_POUT	96h	Read output power	FFFFh	2
PMBUS_REVISION	98h	PMBus compatible revision	22h	1
MFR_ID	99h	DCM controller ID	"VI"	2
MFR_MODEL	9Ah	Internal controller or DCM model	Part Number	18
MFR_REVISION	9Bh	Internal controller or DCM revision	FW and HW revision	18
MFR_LOCATION	9Ch	Internal controller or DCM factory location	"AP"	2
MFR_DATE	9Dh	Internal controller or DCM manufacturing date	"YYWW"	4
MFR_SERIAL	9Eh	Internal controller or DCM serial number	Serial Number	16
MFR_VIN_MIN	A0h	Minimum rated input voltage	Varies per DCM	2
MFR_VIN_MAX	A1h	Maximum rated input voltage	Varies per DCM	2
MFR_VOUT_MIN	A4h	Minimum rated output voltage	Varies per DCM	2
MFR_VOUT_MAX	A5h	Maximum rated output voltage	Varies per DCM	2
MFR_IOUT_MAX	A6h	Maximum rated output current	Varies per DCM	2
MFR_POUT_MAX	A7h	Maximum rated output power	Varies per DCM	2
MFR_CONSTANT_CURRENT	E8h	Set DCM current limit threshold	69h	2
MFR_V_I_COMMIT_COMMAND	ECh	Store output voltage trim and current limit threshold in non-volatile memory	N/A	None

Command Structure Overview

Write Byte protocol:

The Host always initiates PMBus® communication with a START bit. All messages are terminated by the Host with a STOP bit. In a write message, the parent sends the child device address followed by a write bit. Once the child acknowledges, the parent proceeds with the command code and then similarly the data byte.



S Start Condition

Sr Repeated start Condition

Rd Read

Wr Write

X Indicated that field is required to have the value of x

A Acknowledge (bit may be 0 for an ACK or 1 for a NACK)

P Stop Condition

From Parent to Child

From Child to Parent

... Continued next line

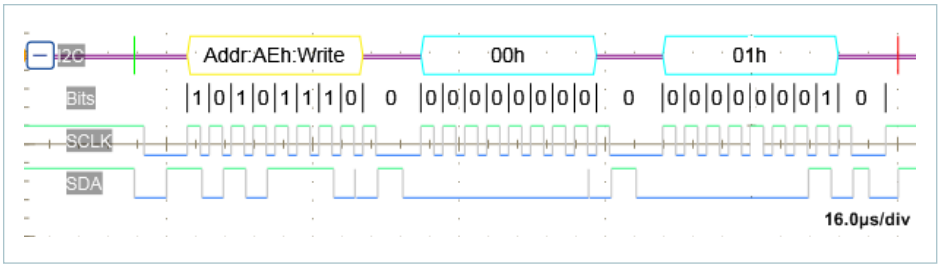
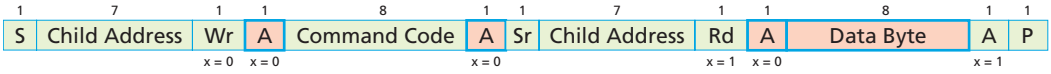


Figure 27 — *PAGE COMMAND (00h), WRITE BYTE PROTOCOL*

Read Byte protocol:

A Read message begins by first sending a Write Command, followed by a REPEATED START Bit and a child Address. After receiving the READ bit, the DCM controller begins transmission of the Data responding to the Command. Once the Host receives the requested Data, it terminates the message with a NACK preceding a stop condition signifying the end of a read transfer.



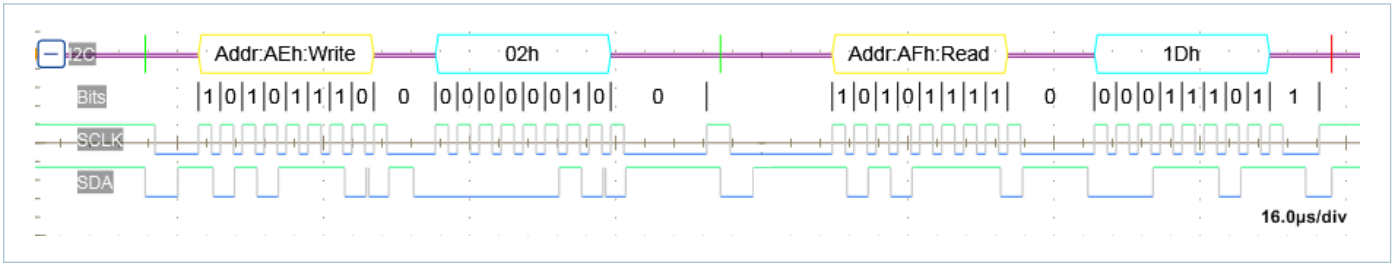
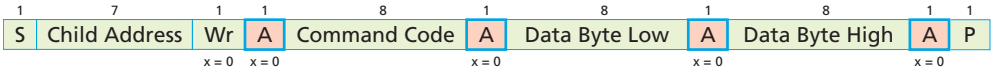


Figure 28 — *ON_OFF_CONFIG COMMAND (02h), READ BYTE PROTOCOL*

Write Word protocol:

When transmitting a word, the lowest order byte leads the highest order byte. Furthermore, when transmitting a Byte, the least significant bit (LSB) is sent last. Refer to System Management Bus (SMBus) specification version 2.0 for more details.

Note: Extended command and Packet Error Checking Protocols are not supported.



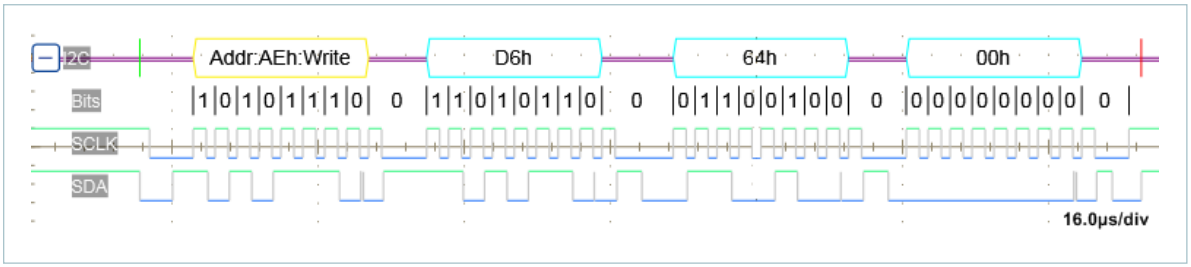
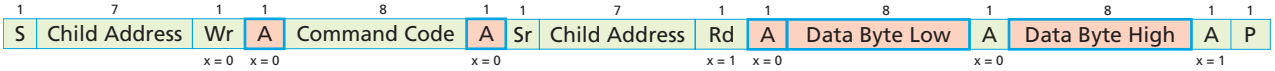


Figure 29 — *TON_DELAY COMMAND (60h)_WRITE WORD PROTOCOL*

Read Word protocol:



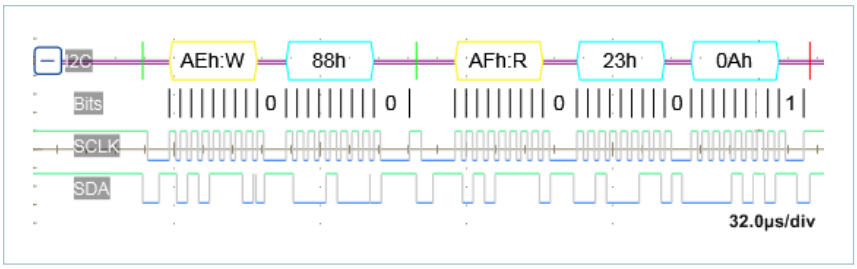
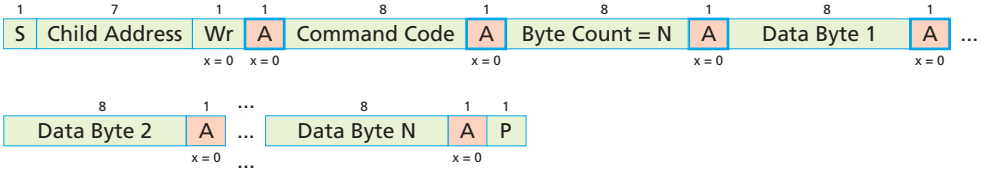


Figure 30 — *MFR_VIN_MIN COMMAND (A0h)_READ WORD PROTOCOL*

Write Block protocol:



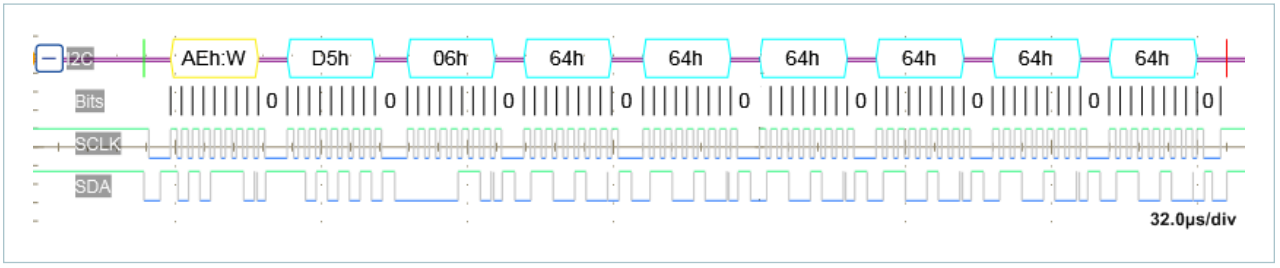
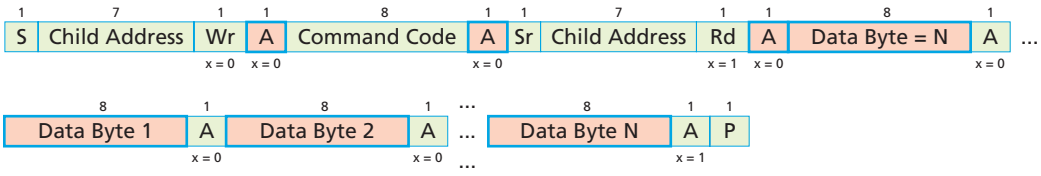


Figure 31 — *SET_ALL_THRESHOLDS COMMAND (D5h)_WRITE BLOCK PROTOCOL*

Read Block protocol:



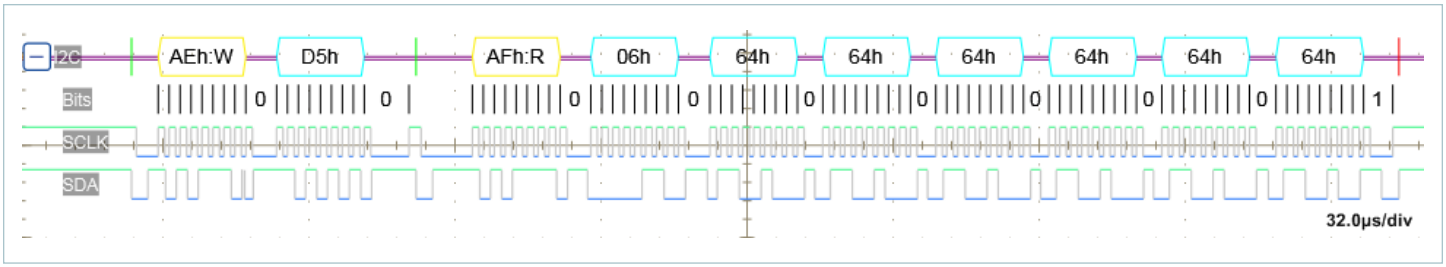
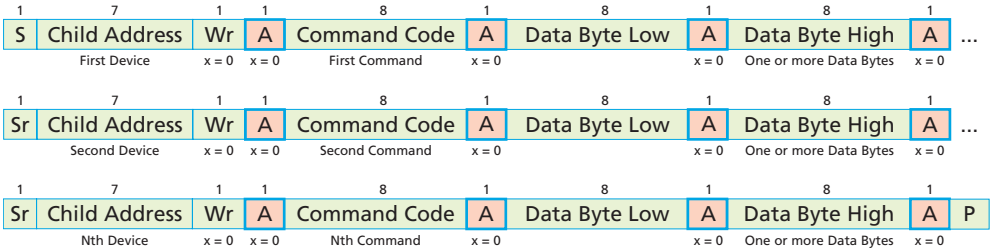


Figure 32 — *SET_ALL_THRESHOLDS COMMAND (D5h)_READ BLOCK PROTOCOL*

Write Group Command protocol:



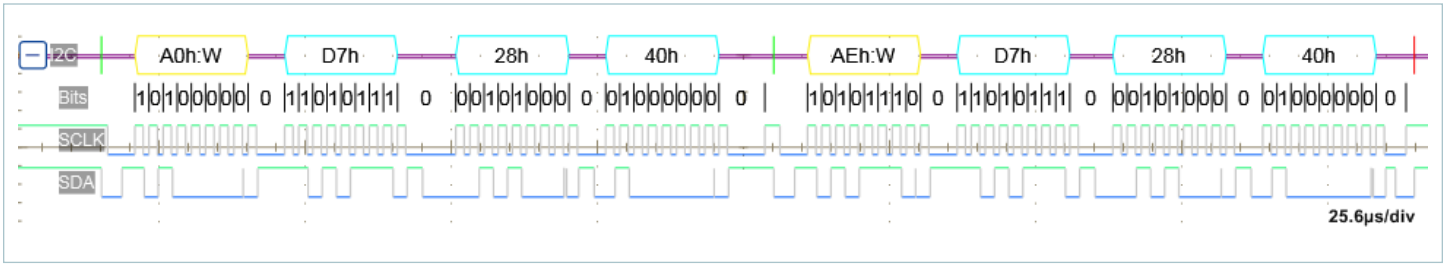


Figure 33 — *DISABLE_FAULT COMMAND (D7h)_WRITE*

Note that only one command per device is allowed in a group command.

Supported Commands Transaction Type

A direct communication to the DCM controller and a simulated communication to non-PMBus® devices is enabled by a page command. Supported command access privileges with a pre-selected PAGE are defined in the following table. Deviation from this table generates a communication error in STATUS_CML register.

Command	Code	PAGE Data Byte Access Type	
		00h	01h
PAGE	00h	R/W	R/W
OPERATION	01h	R	R/W
CLEAR_FAULTS	03h	W	W
CAPABILITY	19h	R	
VOUT_MODE	20h	R	R
VOUT_COMMAND	21h		R/W
STATUS_BYTE	78h	R/W	R
STATUS_WORD	79h	R	R
STATUS_VOUT	7Ah	R	R/W
STATUS_IOUT	7Bh	R	R/W
STATUS_INPUT	7Ch	R	R/W
STATUS_TEMPERATURE	7Dh	R	R/W
STATUS_CML	7Eh	R/W	
STATUS_MFR_SPECIFIC	80h	R/W	R/W
READ_VIN	88h		R
READ_VOUT	8Bh		R
READ_IOUT	8Ch	R	R
READ_TEMPERATURE_1	8Dh	R	R
READ_POUT	96h	R	R
PMBUS_REVISION	98h	R	
MFR_ID	99h	R	
MFR_MODEL	9Ah	R	R
MFR_REVISION	9Bh	R	R
MFR_LOCATION	9Ch	R	R
MFR_DATE	9Dh	R	R
MFR_SERIAL	9Eh	R	R
MFR_VIN_MIN	A0h	R	R
MFR_VIN_MAX	A1h	R	R
MFR_VOUT_MIN	A4h	R	R
MFR_VOUT_MAX	A5h	R	R
MFR_IOUT_MAX	A6h	R	R
MFR_POUT_MAX	A7h	R	R
MFR_CONSTANT_CURRENT	E8h		R/W
MFR_V_I_COMMIT_COMMAND	ECh		W

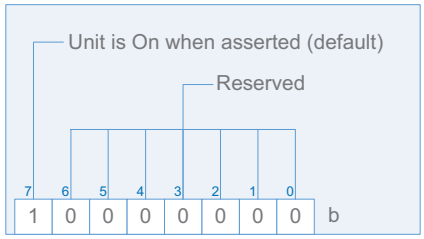
Page Command (00h)

The page command data byte of 00h prior to a command call will address the controller-specific data and a page data byte of 01h would address the DCM.

Data Byte	Description
00h	DCM controller
01h	DCM

OPERATION Command (01h)

The OPERATION command can be used to turn on and off DCM.



This command accepts only two data values: 00h and 80h. If any other value is sent the command will be rejected and a CML Data error will result.

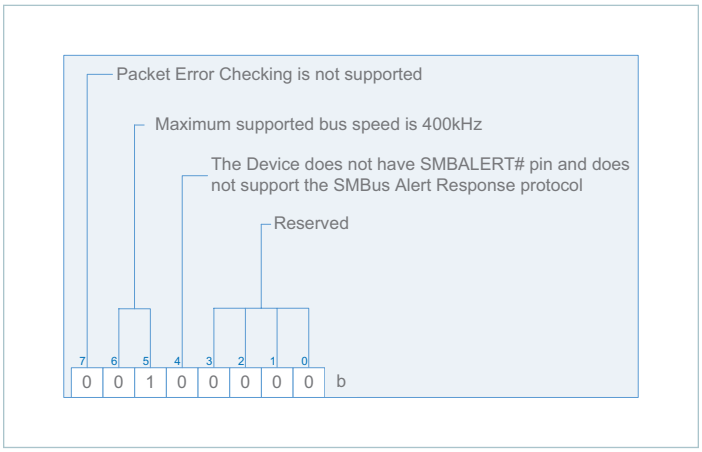
Data Byte	Description
0x80	Turn ON
0x00	Turn OFF

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted once cleared. All faults are latched once asserted in the DCM controller. Registered faults will not be cleared when shutting down the DCM powertrain by sending the OPERATION command.

CAPABILITY Command (19h)

The DCM returns a default value of 20h. This value indicates that the PMBus® frequency supported is up to 400kHz and that both Packet Error Checking (PEC) and SMBALERT# are not supported.



VOUT_MODE Command (20h)

The command returns the information about the mode used for all the output voltage related commands. DCM uses DIRECT Mode (40h) for all the output voltage related commands.

VOUT_COMMAND (21h)

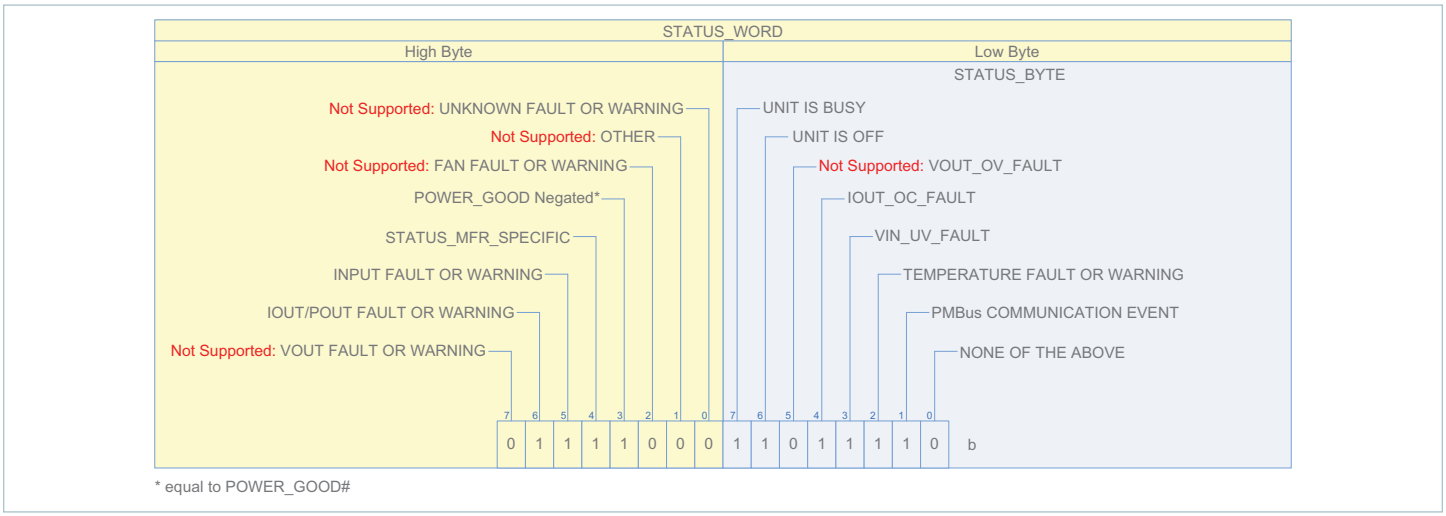
This command sets the output voltage of device to the commanded value.

Any values outside the device output voltage range sent by host will be rejected,will not override the current value and will set the Unsupported data bit in STATUS_CML.

This command uses DIRECT mode and following format:

$$V_{OUT\_SET\_POINT\_ACTUAL} = V_{OUT\_SET\_POINT\_SET} \bullet 10^{-2}\ (Volts)$$

STATUS_BYTE (78h) and STATUS_WORD (79h)



All fault or warning flags, if set, will remain asserted until cleared by the host or once DCM power is removed. This includes undervoltage fault, overvoltage fault, overcurrent fault, overtemperature fault, undertemperature fault, communication faults and analog controller shut-down fault.

Asserted status bits in all status registers, with the exception of STATUS_WORD and STATUS_BYTE, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Refer to the PMBus® Power System Management Protocol Specification – Part II – Revision 1.3 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set, when the DCM is not in the active state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared, when the DCM is in the enabled state, after the powertrain is activated allowing for soft-start to elapse.

POWER_GOOD# and OFF bits cannot be cleared as they always reflect the current state of the device.

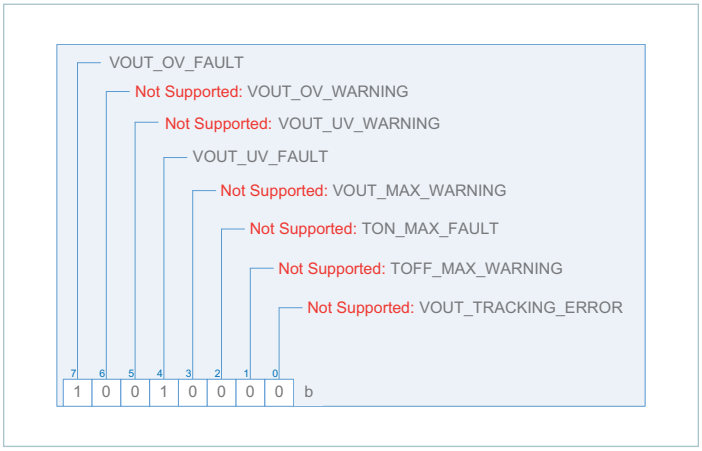
The Busy bit can be cleared using CLEAR_FAULTS Command (03h) or by writing data value (40h) to PAGE (00h) using the STATUS_BYTE (78h).

Fault reporting, such as SMBALERT# signal output, and host notification by temporarily acquiring bus parent status is not supported.

If the DCM controller is powered through VDDE, it will retain the last telemetry data and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard, which requires that status bits remain set until specifically cleared. Note that in the case where the DCM V_{IN} is lost, the status will always indicate an undervoltage fault, in addition to any other fault that occurred.

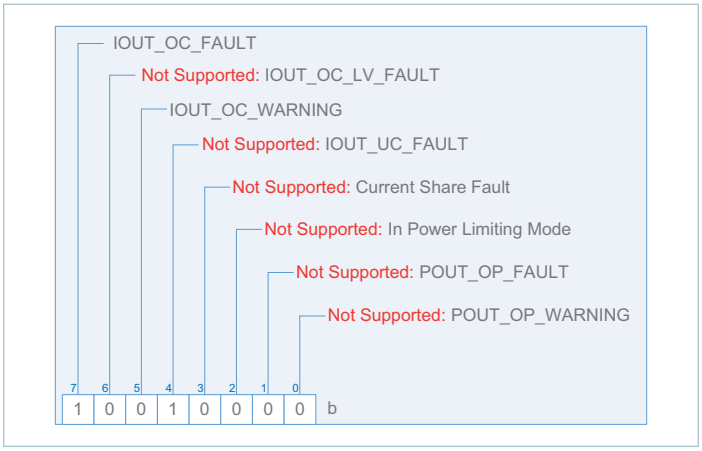
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_VOUT (7Ah)



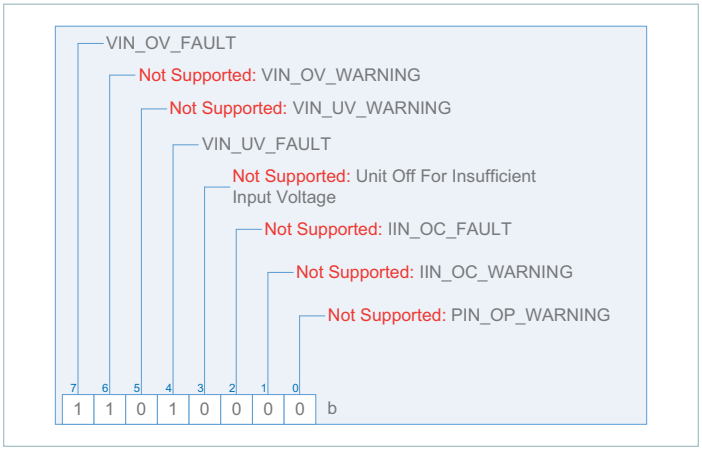
Unsupported bits are indicated above. A one indicates a fault.

STATUS_IOUT (7Bh)



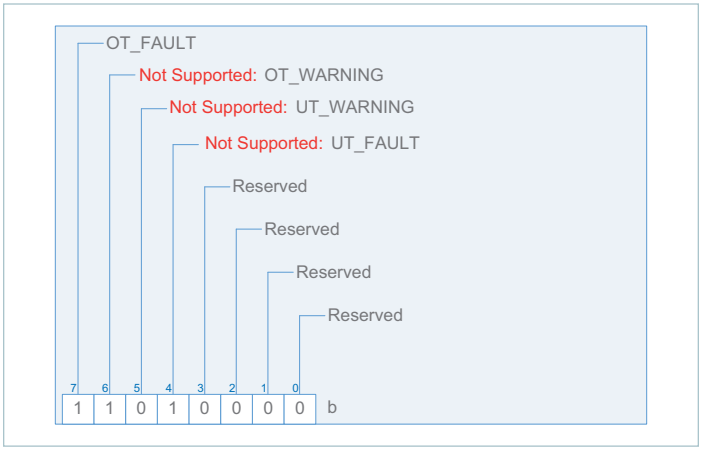
Unsupported bits are indicated above. A one indicates a fault.

STATUS_INPUT (7Ch)



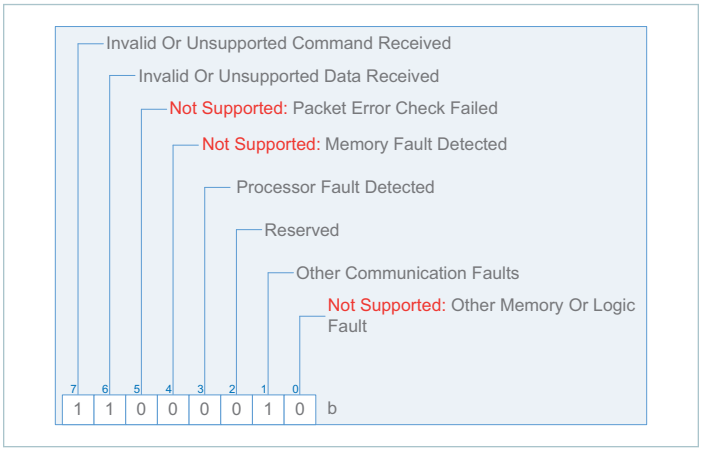
Unsupported bits are indicated above. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unsupported bits are indicated above. A one indicates a fault.

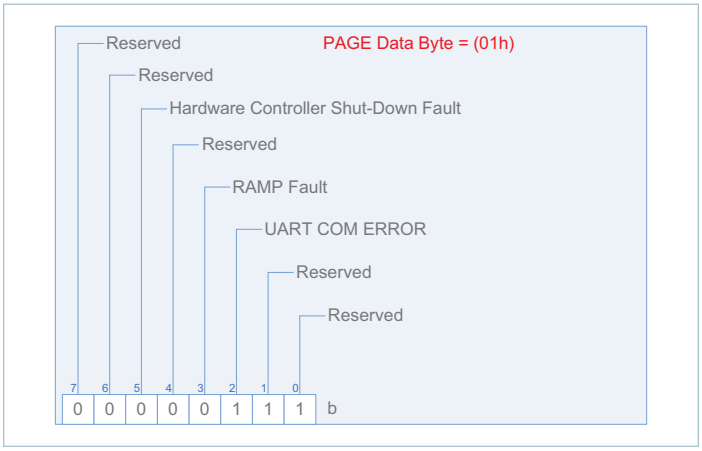
STATUS_CML (7Eh)



Unsupported bits are indicated above. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus® command or data or other communication fault occurs.

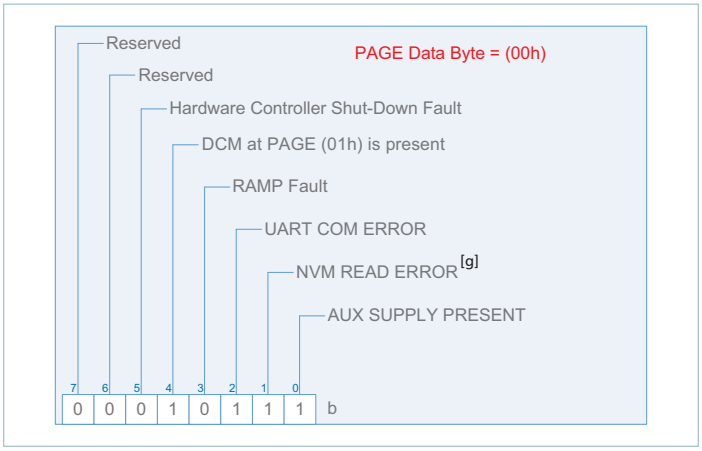
STATUS_MFR_SPECIFIC (80h)



The DCM in a VIA package has hardware protections and supervisory protections. The hardware controller provides an additional layer of protection and has the fastest response time. The Hardware Controller Shut-Down Fault, when asserted, indicates that at least one of the powertrain protection faults is triggered.

The DCM UART is designed to operate with the DCM controller UART. If the DCM UART CML is asserted, it may indicate a hardware or connection issue between both internal devices.

The RAMP Fault bit, if asserted, indicates start of voltage ramp failure.



[g] Non-volatile memory read error.

When PAGE COMMAND (00h) data byte is equal to (00h), Hardware Controller Shut-Down Fault, RAMP fault and DCM UART CML bit will return DCM faults. The DCM UART CML will also be asserted if active DCM stops responding. The DCM must communicate at least once to the DCM controller in order to trigger this FAULT. The DCM UART CML can be cleared using PAGE (00h) CLEAR_FAULTS (03h) Command.

NVM READ ERROR is asserted when the DCM controller has an error reading non-volatile memory on power-up.

AUX SUPPLY PRESENT bit indicates that the DCM controller is powered up by external bias power.

READ_VIN Command (88h)

If PAGE data byte is equal to (01h) command will return DCM's value of input voltage in the following format:

$$V_{IN\_ACTUAL} = V_{IN\_REPORTED} \bullet 10^{-1}\ (Volts)$$

READ_VOUT Command (8Bh)

If PAGE data byte is equal to (01h) command will return DCM's output voltage in the following format:

$$V_{OUT\_ACTUAL} = V_{OUT\_REPORTED} \bullet 10^{-2}\ (Volts)$$

READ_IOUT Command (8Ch)

If PAGE data byte is equal to (00h or 01h) command will return DCM's output current in the following format:

$$I_{OUT\_ACTUAL} = I_{OUT\_REPORTED} \bullet 10^{-2}\ (Amps)$$

READ_TEMPERATURE_1 Command (8Dh)

If PAGE data byte is equal to (00h or 01h) command will return DCM's temperature in the following format:

$$T_{ACTUAL} = \pm T_{REPORTED}\ (^{o}C)$$

READ_POUT Command (96h)

If PAGE data byte is equal to (00h or 01h) command will return DCM's output power in the following format:

$$P_{OUT\_ACTUAL} = P_{OUT\_REPORTED} \bullet 10^{-1}(W)$$

MFR_VIN_MIN Command (A0h), MFR_VIN_MAX Command (A1h), MFR_VOUT_MIN Command (A4h), MFR_VOUT_MAX Command (A5h), MFR_IOUT_MAX Command (A6h), MFR_POUT_MAX Command (A7h)

These values are set by the factory and indicate the device input output voltage and output current range and output power capacity. Information can be accessed with either PAGE (00h) or (01h).

The DCM controller will report rated DCM input voltage minimum and maximum in volts, output voltage minimum and maximum in volts, output current maximum in Amperes and output power maximum in watts.

MFR_CONSTANT_CURRENT COMMAND (E8h)

This command sets the value of DCM current limit threshold as percentage of full load. The DCM will enter constant current operation when a load is connected that exceeds the specified current limit threshold.

Valid values are in the range of 00h – 69h (0 – 105% rated current).

$$I_{OUT\_VALUE\_ACTUAL} = I_{OUT\_VALUE\_SET} \bullet 10^{-2}\ Full\ Load\ (Amps)$$

The constant-current behavior of the DCM can be disabled by entering any value greater than 69h. When disabled, MFR_CONSTANT_CURRENT command will return 82h (130%). In this mode the powertrain will cease switching operation in the event of an overcurrent condition that exceeds the hardware protection threshold $I_{OUT\text{-}CL}$.

MFR_V_I_COMMIT_COMMAND Command (ECh)

This command stores the values of the output voltage set point VOUT_COMMAND (21h) and current limit threshold MFR_CONSTANT_CURRENT (E8h) in non-volatile memory. The stored values become the default voltage setpoint and current limit threshold upon recycling the DCM input voltage.

MFR_V_I_COMMIT_COMMAND is a block command and takes 0 bytes of data.

If enabled, the DCM powertrain will be momentarily disabled while writing to non-volatile memory and will automatically restart once the write sequence is completed.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the DCM.

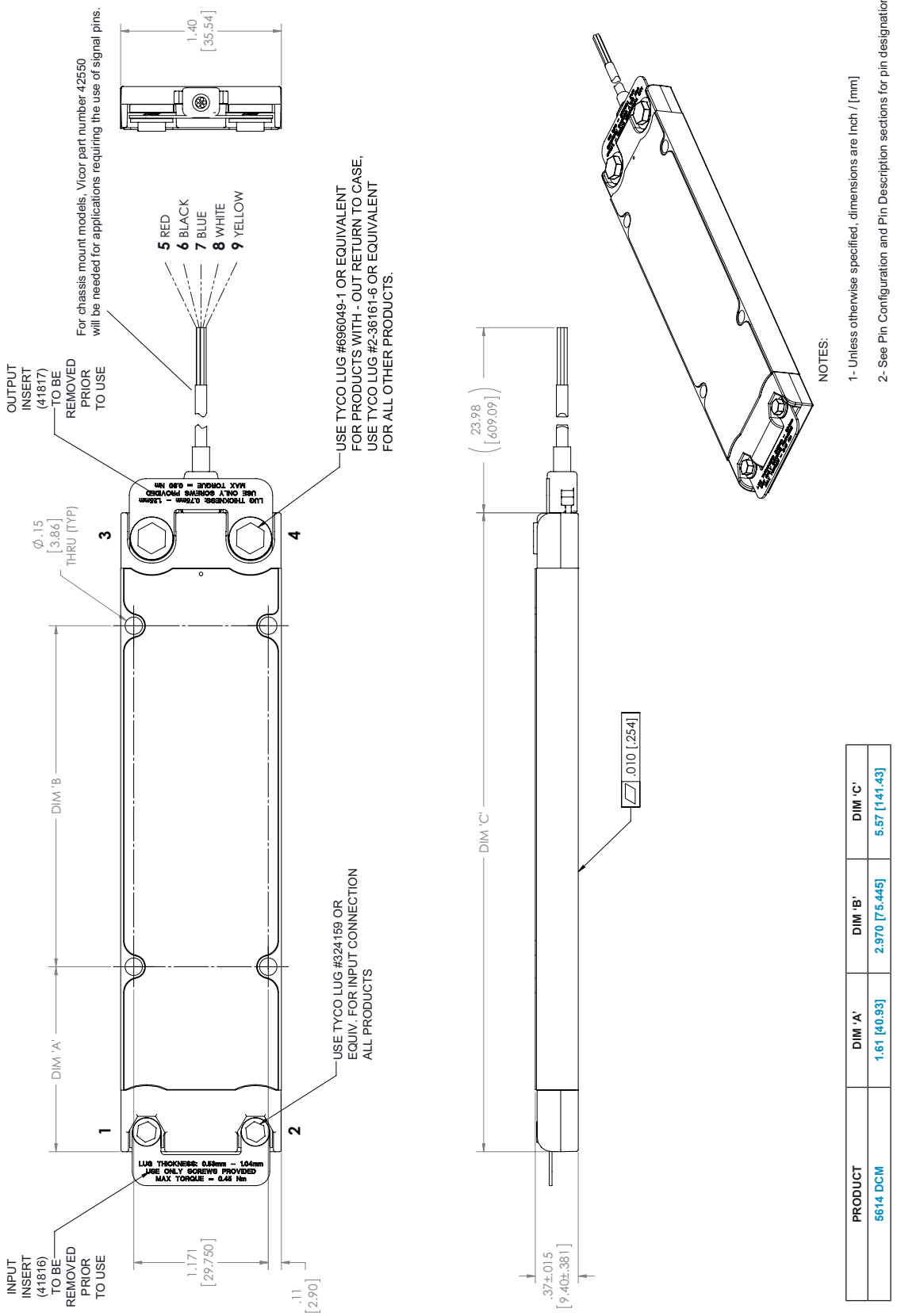
Section	Description	Response to Host		Status Byte	Status CML		Notes
		NACK	FFh	CML	Other Fault	Unsupported Data	
10.8.1	Corrupted Data						No response; PEC not supported
10.8.2	Sending too few bits			X	X		
10.8.3	Reading too few bits			X	X		
10.8.4	Host sends or reads too few bytes			X	X		
10.8.5	Host sends too many tytes	X		X		X	
10.8.6	Reading too many bytes		X	X	X		
10.8.7	Device busy	X	X				Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

Data Content Faults Implementation

This section describes data content faults as implemented in the DCM.

Section	Description	Response to Host	Status Byte	Status CML			Notes
		NACK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Inproperly set read bit in the address byte	X	X	X			
10.9.2	Unsupported command code	X	X		X		
10.9.3	Invalid or unsupported data		X			X	
10.9.4	Data out of range		X			X	
10.9.5	Reserved bits						No response; not a fault

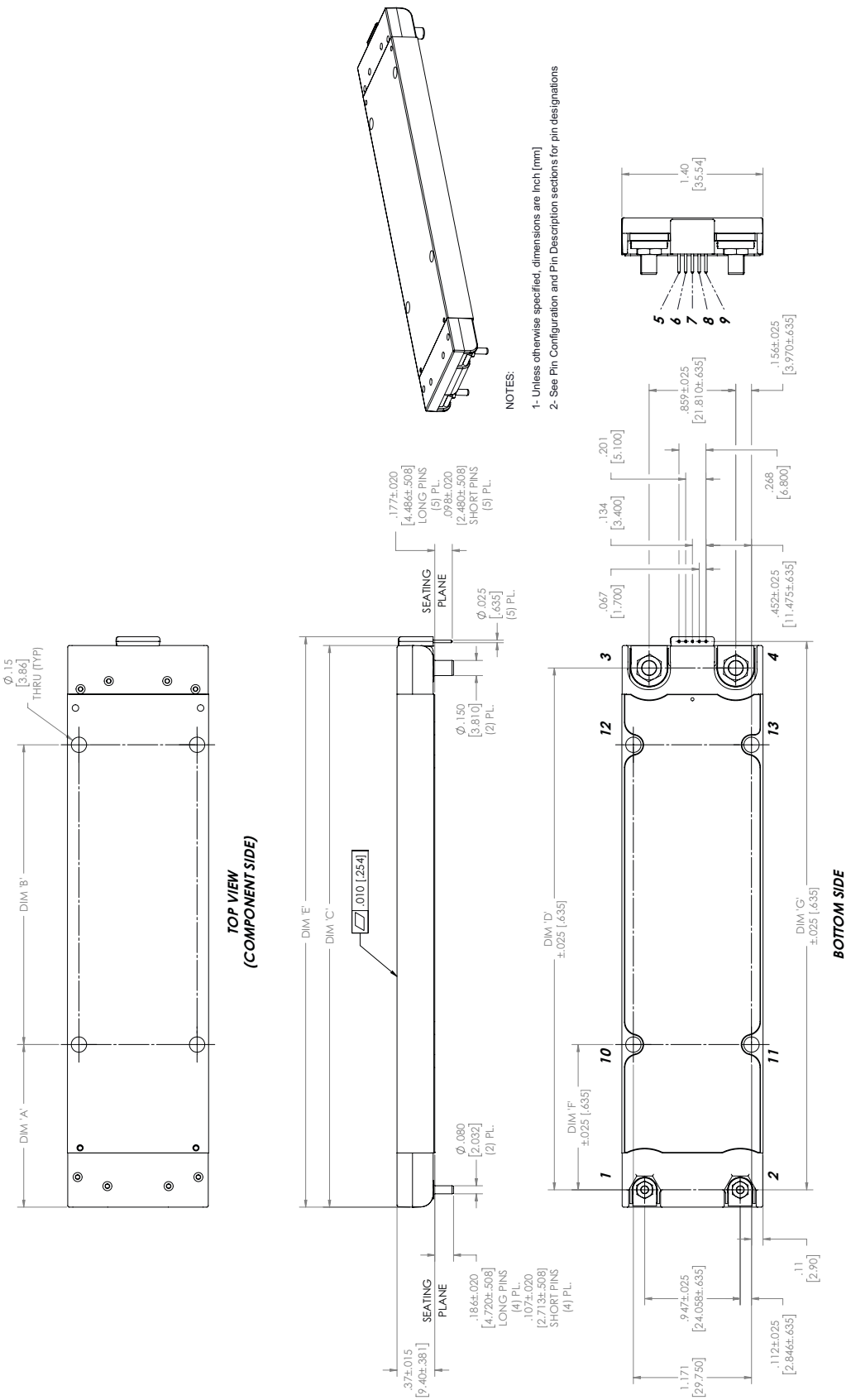
DCM in VIA Package Chassis (Lug) Mount Package Mechanical Drawing



PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'
5614 DCM	1.61 [40.93]	2.970 [75.445]	5.57 [141.43]

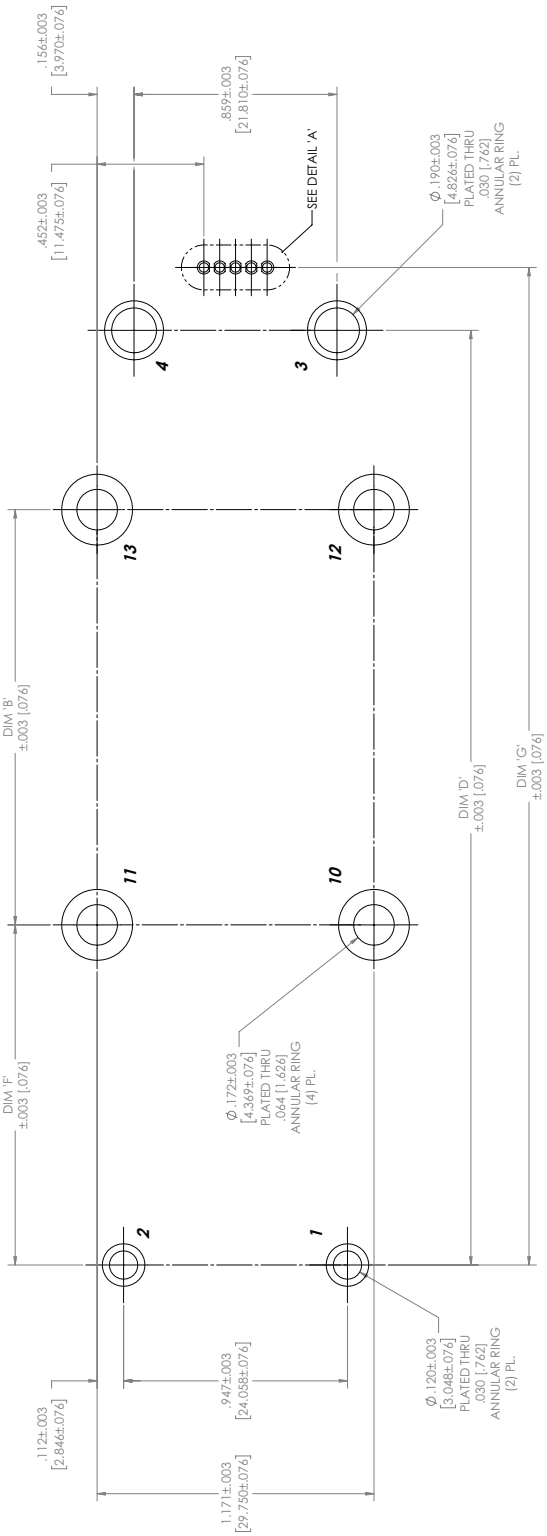
DCM in VIA Package PCB (Board) Mount Package Mechanical Drawing

PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'E'	DIM 'F'	DIM 'G'
5614 DCM	1.61 [40.93]	2.970 [75.445]	5.57 [141.437]	5.171 [131.337]	5.65 [143.58]	1.439 [36.554]	5.434 [138.017]

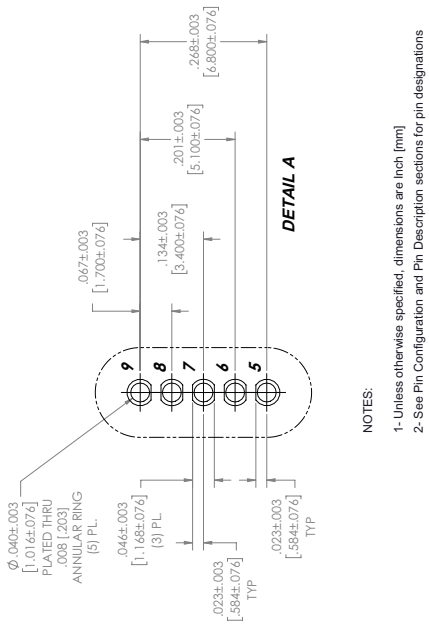


DCM in VIA Package PCB (Board) Mount Package Recommended Hole Pattern

PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'E'	DIM 'F'	DIM 'G'
5614 DCM	1.61 [40.93]	2.970 [75.445]	5.57 [141.437]	5.171 [131.337]	5.65 [143.58]	1.439 [36.554]	5.434 [138.017]



RECOMMENDED HOLE PATTERN (COMPONENT SIDE)



DETAIL A

NOTES:

1- Unless otherwise specified, dimensions are Inch [mm]

2- See Pin Configuration and Pin Description sections for pin designations

Revision History

Revision	Date	Description	Page Number(s)
1.0	03/04/20	Initial release	n/a
1.1	06/29/20	Updated pin functions and design guidelines descriptions for trim Added specification of output voltage for internal microcontroller reset, updated TR and VDDE signal characteristics Updated timing diagrams	3, 20, 21 7, 8 12, 13
1.2	08/11/20	Updated terminology	26, 28, 29, 30, 33
1.3	06/08/23	Added new configuration: DCM5614BD0H36K3TA9	4, 21, 26 – 28

Note: pages added in Rev 1.1, 1.3.

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6,788,033; 7,154,250; 6,930,893; 7,145,786; 7,420,825; 6,788,033; 6,930,893; 7,145,786; 7,154,250; 7,420,825; 7,561,446; 7,782,639; 7,920,391; 8,427,269; 8,669,744; 8,966,747; 9,387,633; 9,508,485; 9,516,761; 9,712,055; 9,899,924; 9,936,580; 9,967,984; 10,050,519; 10,135,334; 10,398,040; D837,734 and other patents pending

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